UC25LD40IB

Ultra Low Power, 4M-bit

Serial Standard and Dual I/O Flash Memory Datasheet

Key Features

- Wide supply range from 1.65V to 2.0V for Read, Erase and Program
- Ultra-Low Power consumption for Read, Erase and Program
- x1, x2 Multi I/O Support
- High reliability with 100K cycling endurance and 20-year data retention

Nanjing UCUN Technology, Inc.

Contents

1. GENERAL DESCRIPTIONS

The UC25LD40IB (4M-Bit) serial flash supports the standard Serial Peripheral Interface (SPI), and supports the Dual SPI: Serial Clock, Chip Select, Serial Data I/O0 (SI), I/O1 (SO), I/O2. The Dual output data is transferred with Maximum speed of 130Mbits/s.

2. FEATURES

- **SPI Flash Memories**
  - Densities: 4Mbit
  - Standard SPI: SCLK, /CS, SI, SO
  - Dual SPI: SCLK, /CS, IO0, IO1

- **Highest Performance Serial Flash**
  - 80MHz for fast read
  - Dual I/O Data transfer up to 130Mbits/s
  - Minimum 100,000 Program/Erase Cycles
  - More than 20-year data retention

- **Low Power Consumption**
  - Single 1.65V to 2.0V supply
  - 0.5μA standby current
  - 0.5μA deep power down current
  - 1.5mA active read current at 33MHz
  - 3.0mA active program or erase current

- **Flexible Architecture**
  - Uniform 256-byte Page Erase
  - Uniform 4K-byte Sector Erase
  - Uniform 32/64K-byte Block Erase
  - Program 1 to 256 byte per programmable page

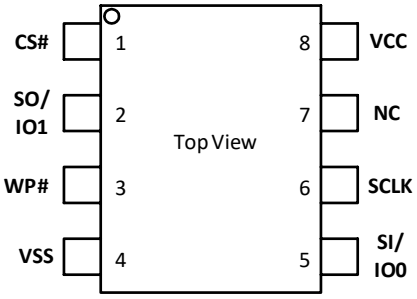
- **Fast Program and Erase Speed**
  - 2ms page program time
  - 15ms page erase time
  - 15ms 4K-byte sector erase time
  - 15ms 32K/64K-byte block erase time

- **Advanced Security Features**
  - 128-Bit Unique ID for each device
  - 2*256-Byte Security Registers with OTP Locks

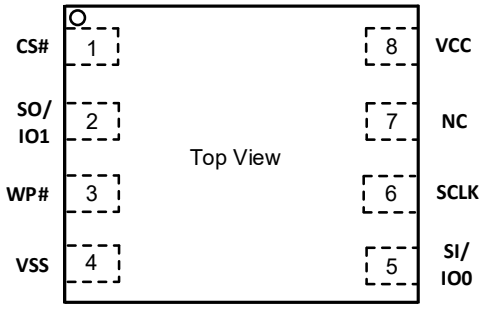
- **Package Information**
  - SOP8
  - USON8 (3 x2 mm)
  - TSSOP8
  - KGD

3. PIN DEFINITION

3.1 PIN CONFIGURATION



8 - LEAD VSOP/SOP



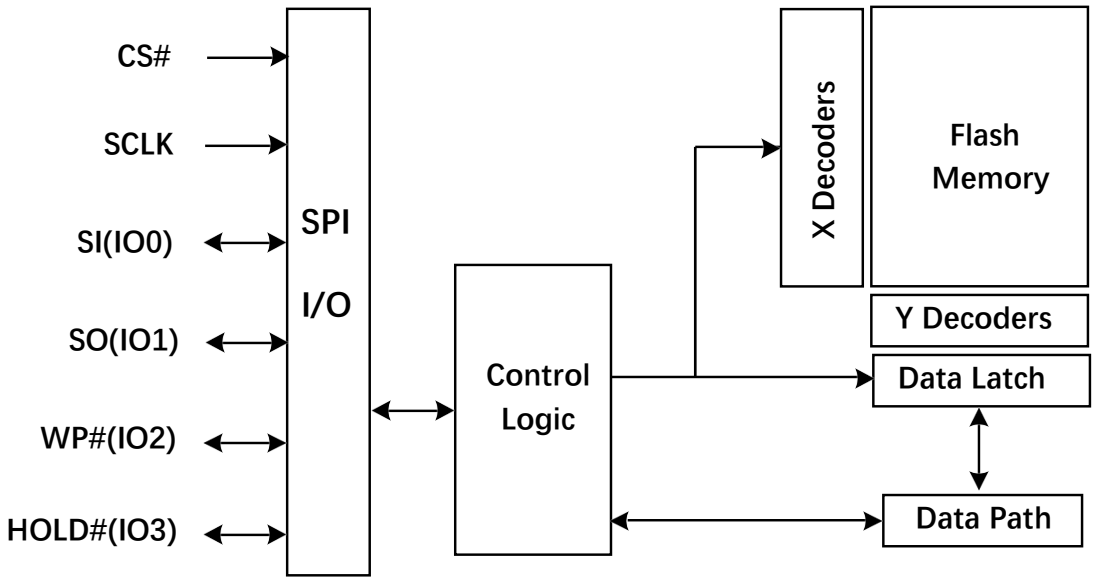
8 - LEAD WSON/USON

3.2 PIN DESCRIPTION

Table-1. Pin Definition

Pin No.	Pin Name	I/O	Description
1	CS#	I	Chip Select Input
2	SO (IO1)	I/O	Data Output (Data Input Output 1)
3	WP#	I	Write Protect Input
4	VSS		Ground
5	SI (IO0)	I/O	Data Input (Data Input Output 0)
6	SCLK	I	Serial Clock Input
7	NC		No Connection
8	VCC		Power Supply

4. BLOCK DIAGRAM



5. MEMORY ORGANIZATION

Table-2.0 UC25LD40IB Array Organization

Each device has	Each block has	Each sector has	Each page has	
512K	64/32K	4K	256	Bytes
2K	256/128	16	-	Pages
128	16/8	-	-	Sectors
8/16	-	-	-	Blocks

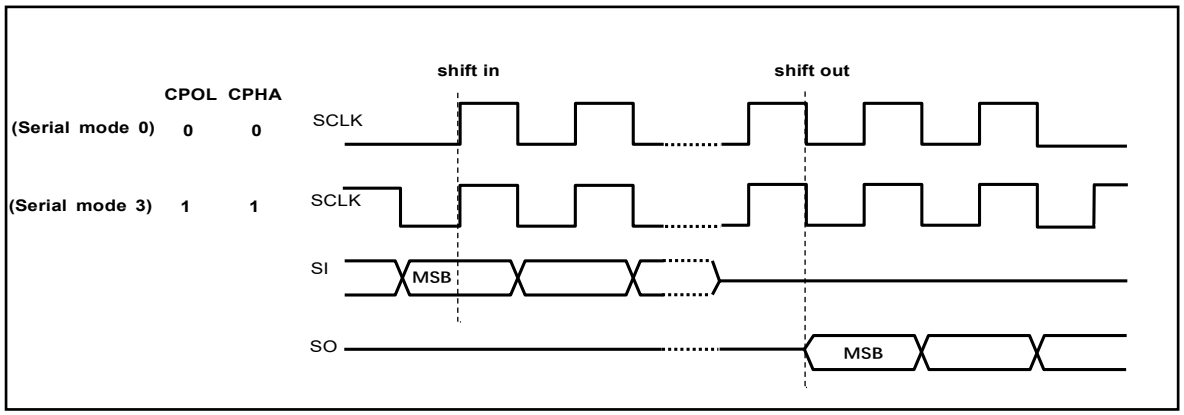
Table-3.0 UC25LD40IB Uniform Block Sector Architecture

Block (64K-byte)	Block (32K-byte)	Sector (4K-byte)	Address Range	
7	14~15	127	07F000H	07FFFFH
		……	……	……
		112	070000H	070FFFH
6	12~13	111	06F000H	06FFFFH
		……	……	……
		96	060000H	060FFFH
……	……	……	……	……
		……	……	……
		……	……	……
1	2~3	31	01F000H	01FFFFH
		……	……	……
		16	010000H	010FFFH
0	0~1	15	00F000H	00FFFFH
		……	……	……
		0	000000H	000FFFH

6. DEVICE OPERATION

1. Before a command is issued, the status register should be checked to ensure the device is ready for the intended operation.
2. When an incorrect command is input, the device enters standby mode and remains in standby mode until the next CS# falling edge. In standby mode, the SO pin of the device is in High-Z.
3. When the correct command is input, the device enters active mode and remains in active mode until the next rising edge of CS#.
4. For standard single data rate serial mode, input data is latched on the rising edge of Serial Clock (SCLK) and data is shifted out on the falling edge of SCLK. The difference between Serial mode 0 and mode 3 is shown in Figure-1.

Figure-1. Serial Modes Supported (for Normal Serial Mode)



Standard SPI

The UC25LD40IB features a serial peripheral interface on 4 signals: Serial Clock (SCLK), Chip Select (CS#), Serial Data Input (SI) and Serial Data Output (SO). Both SPI bus mode 0 and 3 are supported. Input data is latched on the rising edge of SCLK and is data shifted out on the falling edge of SCLK.

Dual SPI

The UC25LD40IB supports Dual SPI operation when using the “Dual Output Fast Read” (3BH) commands. The command allow data to be transferred to or from the device at twice the rate of the standard SPI. When using the Dual SPI command, the SI and SO pins become bidirectional I/O pins: IO0 and IO1.

7. STATUS REGISTER

Table-4. Status Register

S15	S14	S13	S12	S11	S10	S9	S8
(R)	(R)	(R)	LB2	LB1	(R)	(R)	(R)
Reserved	Reserved	Reserved	Non-volatile OTP		Reserved	Reserved	Reserved

S7	S6	S5	S4	S3	S2	S1	S0
SRP	(R)	(R)	BP2	BP1	BP0	WEL	WIP
Non-volatile	Reserved	Reserved	Non-volatile			Read-only	Read-only

The status and control bits of the Status Register are as follows:

WIP bit

The Write in Progress (WIP) bit indicates whether the device is busy executing a program/erase/write status register operation. When the Write in Progress (WIP) bit is set to 1, a program/erase/write status register operation is in progress. When the Write in Progress (WIP) bit is set to 0, the device does not have a program/erase/write status register operation in progress.

WEL bit

The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch. When set to 1, the internal Write Enable Latch is set, when set to 0 the internal Write Enable Latch is reset, and no Write Status Register, Program or Erase command is accepted.

BP2, BP1, BP0 bits

The Block Protect (BP2, BP1, BP0) bits are non-volatile. They define the size of the area to be software protected against Program and Erase commands. These bits are written with the Write Status Register (WRSR) command. When the Block Protect (BP2, BP1, BP0) bits are set to 1, the relevant memory area (as defined in Table1).becomes protected against Page Program (PP), Sector Erase (SE) and Block Erase (BE) commands. The Block Protect (BP2, BP1, BP0) bits can be written provided that the Hardware Protected mode has not been set. The Chip Erase (CE) command is executed, if the Block Protect (BP2, BP1, BP0) bits are all 0. The default value of BP2:0 are 0s.

SRP bits

The Status Register Protect (SRP) bit operates in conjunction with the Write Protect (WP#) signal. The Status Register Write Protect (SRP) bit and Write Protect (WP#) signal set the device to the Hardware Protected mode. When the Status Register Protect (SRP) bit is set to 1, and Write Protect (WP#) is driven Low. In this mode, the non-volatile bits of the Status Register(SRP, BP2, BP1, BP0) become read-only bits and the Write Status Register (WRSR) instruction is not execution. The default value of SRP is 0.

LB2, LB1 bits

The LB2, LB1 bits are non-volatile One Time Program (OTP) bits in Status Register (S12-S11) that provide the write protect control and status for the Security Registers. The default state of LB2-LB1 is 0, with the security registers unprotected. The LB2-LB1 bits can be set to 1 individually using the Write Register (01H&31H) command. The LB2-LB1 bits are One Time Programmable, once setting to 1, the corresponding Security Registers will become read-only permanently.

8. DATA PROTECTION

During power transition, there may be some false system level signals which result in inadvertent erasure or programming. The device is designed to protect itself from these accidental write cycles.

The state machine will be reset to standby mode automatically during power up. In addition, the control register architecture of the device ensures that the memory contents can only be changed after specific command sequences have completed successfully.

In the following, there are several features to protect the system from the accidental write cycles during VCC power-up and power-down or from system noise.

- Valid command length checking: The command length will be checked whether it is at byte base and completed on byte boundary.
- Write Enable (06H) command: WREN command is required to set the Write Enable Latch bit (WEL) before issuing other commands to change data.
- Software Protection Mode: The Block Protect (BP2, BP1, and BP0) bits define the section of the memory array that can be read but not changed.
- Hardware Protection Mode: WP# going low to protect the BP0~BP2 bits and SRP bits.
- Deep Power-Down Mode: By entering deep power down mode, the flash device is ignores all commands until the Release from Deep Power-Down Mode (B9H) command.

Table-5.0 UC25LD40IB Protected Area Size

Status Register Content			Memory Content			
BP2	**BP1**	**BP0**	**Blocks**	**Addresses**	**Density**	**Portion**
0	0	0	NONE	NONE	NONE	NONE
0	0	1	Sector 0 to 125	000000H-07DFFFH	504KB	Lower126/128
0	1	0	Sector 0 to 123	000000H-07BFFFH	496KB	Lower 124/128
0	1	1	Sector 0 to 119	000000H-077FFFH	480KB	Lower 120/128
1	0	0	Sector 0 to 111	000000H-06FFFFH	448KB	Lower 112/128
1	0	1	Sector 0 to 95	000000H-05FFFFH	384KB	Lower 96/128
1	1	0	Sector 0 to 63	000000H-03FFFFH	256KB	Lower 64/128
1	1	1	All	000000H-07FFFFH	512KB	ALL

9. COMMAND DESCRIPTION

All commands, addresses and data are shifted in and out of the device, beginning with the most significant bit on the first rising edge of SCLK after CS# is driven low. Then, the one-byte command code must be shifted into the device starting with the most significant bit on SI. Each bit is latched on the rising edge of SCLK.

The commands supported by UC25LD40IB are listed in Table-6. Every command sequence starts with a one-byte command code. Depending on the command, this might be followed by address or data bytes, by both or none. CS# must be driven high after the last bit of the command sequence has been completed. For the commands of Read, Fast Read, Read Status Register, Release from Deep Power- Down, and Read Device ID, the shifted-in command sequence is followed by a data-out sequence. All read commands can be completed after any bit of the data-out sequence is shifted out, and then CS# must be driven high to return to deselected status.

For the Page Program (02H), Sector Erase (20H), Half Block Erase (52H), Block Erase (D8H), Chip Erase (C7H or 60H), Write Status Register (01H), Write Enable (06H), Write Disable (04H) or Deep Power-Down (B9H) commands, CS# must be driven high exactly at a byte boundary, otherwise the command is rejected, and is not executed. That means CS# must be driven high when the number of clock pulses after CS# being driven low is an exact multiple of eight. For Page Program, if CS# is driven high at any time the input byte is not a full byte, nothing will happen and WEL will not be reset.

Table-6. Commands (Standard/Dual SPI)

Command Name	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	n-Bytes
Write Enable	06H						
Write Disable	04H						
Write Enable for Volatile Status Register	50H						
Read Status Register-1	05H	(S7-S0)					(continuous)
Read Status Register-2	35H	(S15-S8)					(continuous)
Write Status Register-1	01H	S7-S0					
Write Status Register-1&2	01H	S7-S0	S15-S8				
Write Status Register-2	31H	S15-S8					
Read Data Bytes	03H	A23-A16	A15-A8	A7-A0	(D7-D0)	(Next byte)	(continuous)
Read Data Bytes at Higher Speed	0BH	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	(continuous)
Dual Output Fast Read	3BH	A23-A16	A15-A8	A7-A0	dummy	(D7-D0) (1)	(continuous)
Page Erase	81H	A23-A16	A15-A8	A7-A0			
Sector Erase	20H	A23-A16	A15-A8	A7-A0			
Half Block Erase	52H	A23-A16	A15-A8	A7-A0			
Block Erase	D8H	A23-A16	A15-A8	A7-A0			
Chip Erase	C7/60H						
Page Program	02H	A23-A16	A15-A8	A7-A0	D7-D0	Next byte	continuous
Erase Security Register (2)	44H	A23-A16	A15-A8	A7-A0			
Program Security Register (2)	42H	A23-A16	A15-A8	A7-A0	D7-D0	D7-D0	continuous
Read Security Register (2)	48H	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	(continuous)
Deep Power-Down	B9H						
Release from Deep Power-Down	ABH						
Release from Deep Power-Down, Read Electronic Signature	ABH	dummy	dummy	dummy	(DID7-DID0)		(continuous)
Read Electronic Manufacturer ID & Device ID	90H	dummy	dummy	00H	(MID7-MID0)	(DID7-DID0)	(continuous)
Read Identification	9FH	(MID7-MID0)	(JDID15-JDID8)	(JDID7-JDID0)			(continuous)
Reset Enable	66H						
Reset	99H						
Read Unique ID	4BH	00H	00H	00H	dummy	(UID7- UID0)	(continuous)

Notes:

1. Dual Output data

   IO0 = (D6, D4, D2, D0)

   IO1 = (D7, D5, D3, D1)

2. Security Registers Address:

   Security Register1: A23-A16=00H, A15-A12=1H, A11-A8 = 0000b, A7-A0= Byte Address;

   Security Register2: A23-A16=00H, A15-A12=2H, A11-A8 = 0000b, A7-A0= Byte Address;

Tables of ID Definition:

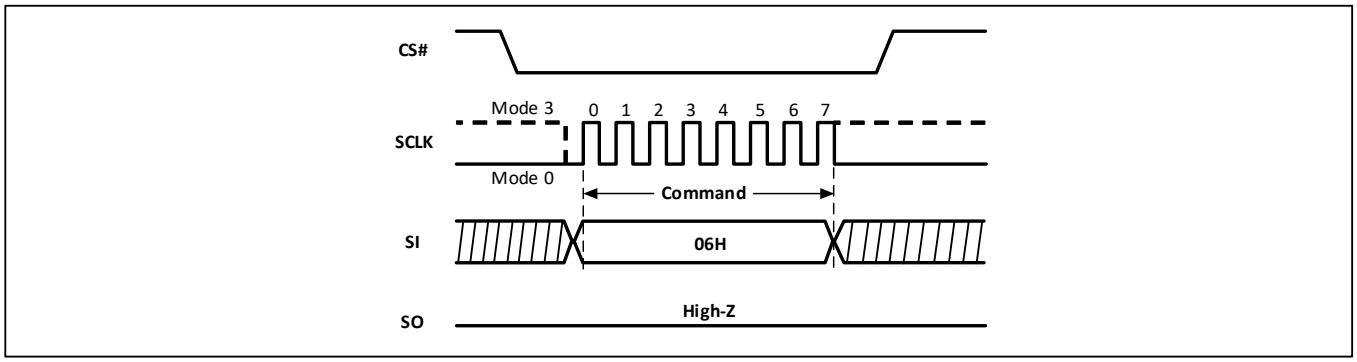
Table-7.0 UC25LD40IB ID Definition

Operation Code	MID7-MID0	ID15-ID8	ID7-ID0
9FH	B3	60	13
90H/92H	B3		12
ABH			12

9.1 Write Enable (WREN) (06H)

The Write Enable (06H) command sets the Write Enable Latch (WEL) bit. The WEL bit must be set prior to every Page Program, Page Erase, Sector Erase, Half Block Erase, Block Erase, Chip Erase, Write Status Register and Erase/Program Security Register command. The WREN command is entered by driving Chip Select (CS#) Low, sending the command code, and then driving CS# High.

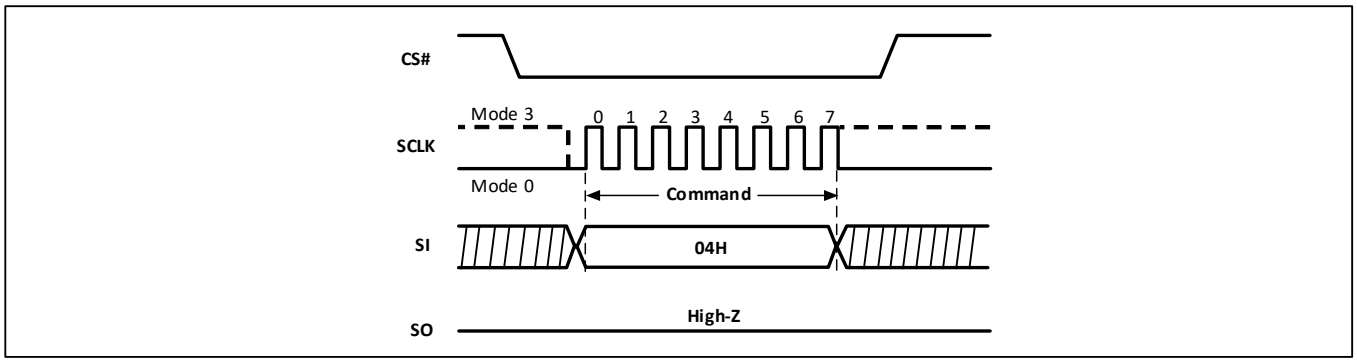
Figure-2. Write Enable Sequence Diagram



9.2 Write Disable (WRDI) (04H)

The Write Disable (04H) command resets the Write Enable Latch (WEL) bit in the Status Register to 0. The WRDI command is entered by driving Chip Select (CS#) low, shifting the command code "04h" into the SI pin and then driving CS# high. Note that the WEL bit is automatically reset after Power-up and upon completion of the Write Status Register, Page Program, Page Erase, Sector Erase, Half Block Erase, Block Erase, Chip Erase, Erase/Program Security Register and Reset commands.

Figure-3. Write Disable Sequence Diagram

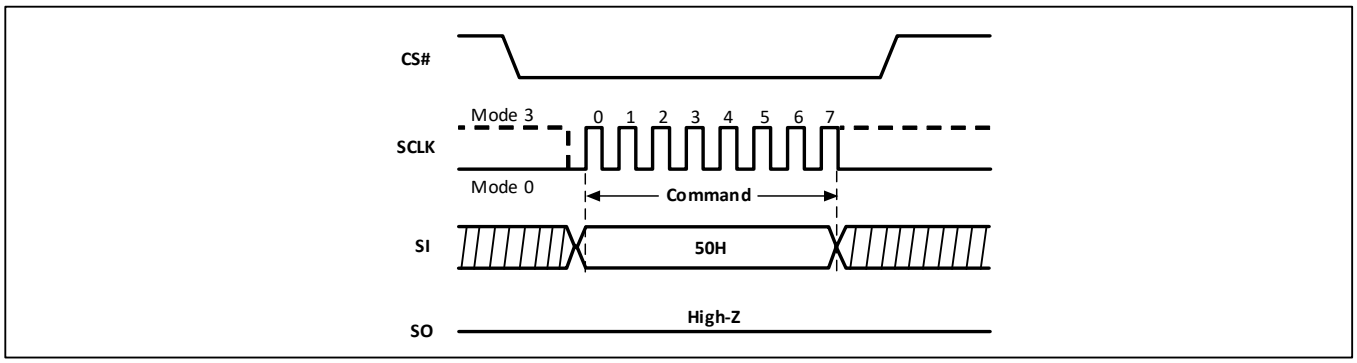


9.3 Write Enable for Volatile Status Register (50H)

The non-volatile Status Register bits can also be written to as volatile bits. During power up reset, the non-volatile Status Register bits are copied to a volatile version of the Status Register that is used during device operation. This provides more flexibility to change the system configuration and memory protection schemes quickly without waiting for the typical non-volatile bit write cycles or affecting the endurance of the Status Register non-volatile bits.

To write the volatile version of the Status Register bits, the Write Enable for Volatile Status Register (50H) command must be issued and immediately followed by the Write Status Register (01H) command. Write Enable for Volatile Status Register command (Figure-4) will not set the Write Enable Latch (WEL) bit, it is only valid for the next Write Status Register command, to change the volatile Status Register bit values.

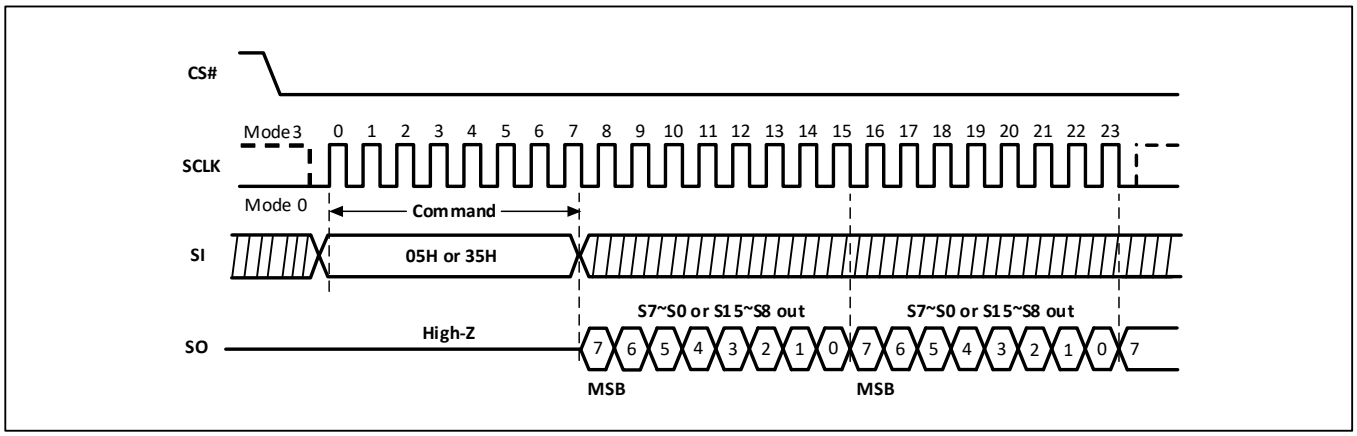
Figure-4. Write Enable for Volatile Status Register Sequence Diagram



9.4 Read Status Register (RDSR) (05H or 35H)

The Read Status Register (05H or 35H) command allows the Status Register to be read. The Status Register may be read at any time, even while a Program, Erase or Write Status Register cycle is in progress. When one of these cycles is in progress, it is recommended to check the Write In Progress (WIP) bit before sending a new command to the device. It is also possible to read the Status Register continuously. For command code “05H”, the SO will output Status Register bits S7~S0. And for command code “35H”, the SO will output Status Register bits S15~S8.

Figure-5. Read Status Register Sequence Diagram



9.5 Write Status Register (WRSR) (01H or 31H)

WRSR can write 8 bits or 16 bits data. The Write Status Register (01H for one byte or two bytes, 31H for one byte only) command allows new values to be written to the Status Register. Command 01H is used to write S7~S0 (one byte) or S15~S0 (two bytes). Command 31H is used to write S15~S8. Before the command can be accepted, a Write Enable (06H) command must previously have been executed. After the Write Enable command has been decoded and executed, the device sets the Write Enable Latch (WEL).
The WRSR command is entered by driving Chip Select (CS#) Low, followed by the command code and the data byte on Data Input (SI).

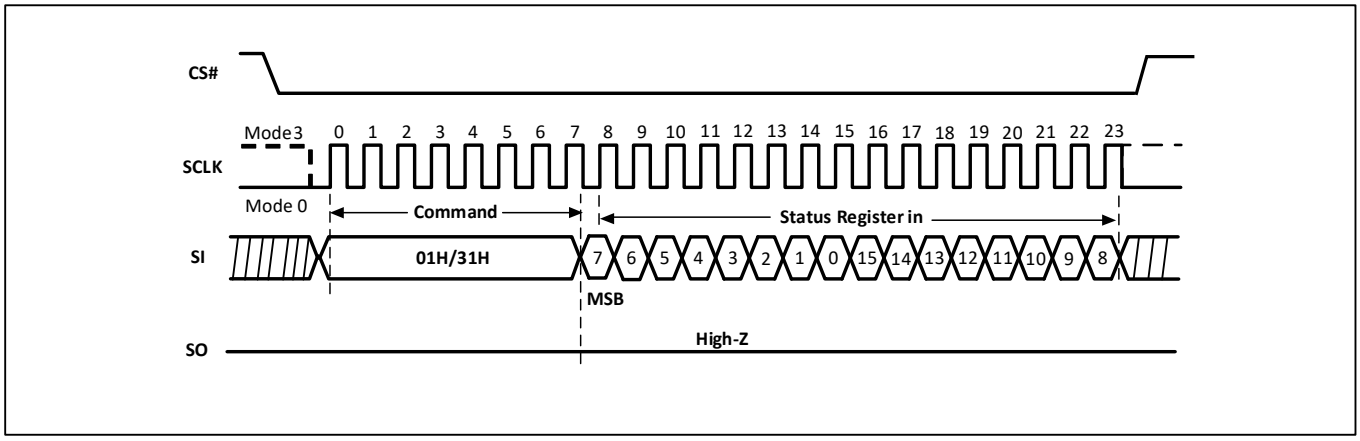
The WRSR command has no effect on S15~S13, S10~S8, S5, S6, S1 and S0 of the Status Register. CS# must be driven high after the sixteenth bit or eighth bit of the data byte has been latched in. If not, the WRSR command is not executed. As soon as CS# is driven High, the self-timed Write Status Register cycle (whose duration is tW) is initiated. While the Write Status Register cycle is in progress, the Status Register may still be read to check the value of the Write In Progress (WIP) bit. The WIP bit is 1 during the self-timed Write Status Register cycle and is 0 when it is completed. When the cycle is completed, the WEL bit is reset.

The WRSR command allows the user to change the values of the Block Protect (BP2, BP1, BP0) bits. The WRSR command also allows the user to set or reset the Status Register Protect (SRP) bits in

accordance with the Write Protect (WP#) signal. The Status Register Protect (SRP) bits and WP# signal allow the device to be put in the Hardware Protection Mode. The WRSR command is not executed once the Hardware Protection Mode is entered.

CS# must go high exactly at the 8bit or 16bit data boundary; otherwise the command will be rejected and not executed. The self-timed Write Status Register cycle time (tW) is initiated as soon as CS# goes high. The WIP bit still can be checked during the Write Status Register cycle is in progress. The WIP is set to 1 during tW and is reset to 0 along with the WEL bit when Write Status Register Cycle is completed.

Figure-6. Write Status Register Sequence Diagram



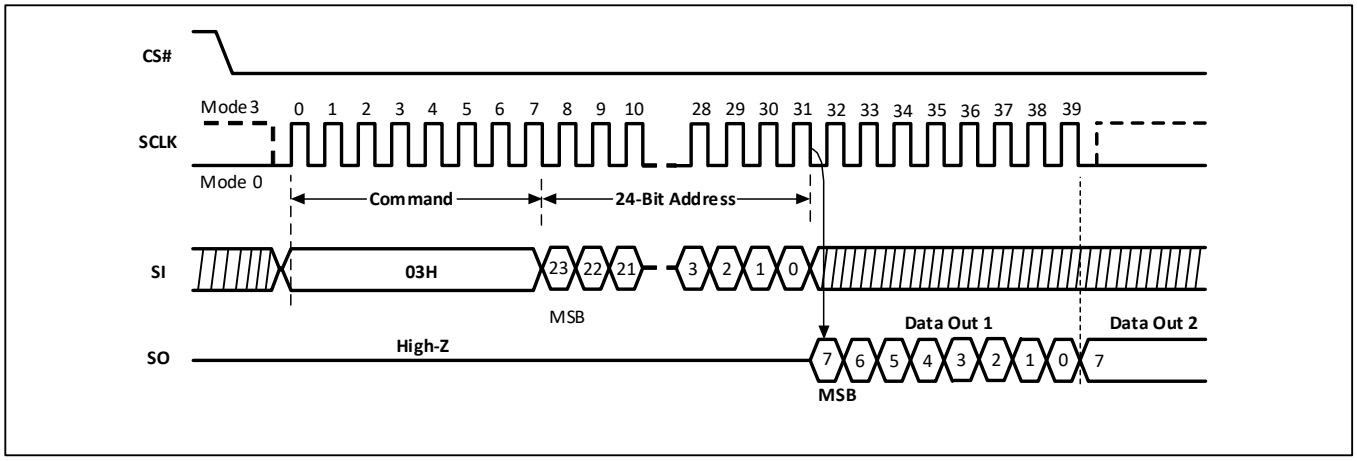
9.6 Read Data Bytes (READ) (03H)

The device is first selected by driving Chip Select (CS#) Low. The command code for the Read Data Bytes (03H) command is followed by a 3-byte address (A23-A0), with each bit latched-in on the rising edge of Serial Clock (SCLK). Then the memory contents, at that address, is shifted out on Data Output (SO), with each bit shifted out at a maximum frequency fR on the falling edge of SCLK.

The command sequence is shown in Figure-7. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The whole memory can, therefore, be read with a single READ command. When the highest address is reached, the address counter rolls over to 000000h, allowing the read sequence to be continued indefinitely.

The READ command is terminated by driving CS# High. CS# can be driven High at any time during data output. Any READ command to the memory array, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure-7. Read Data Bytes Sequence Diagram



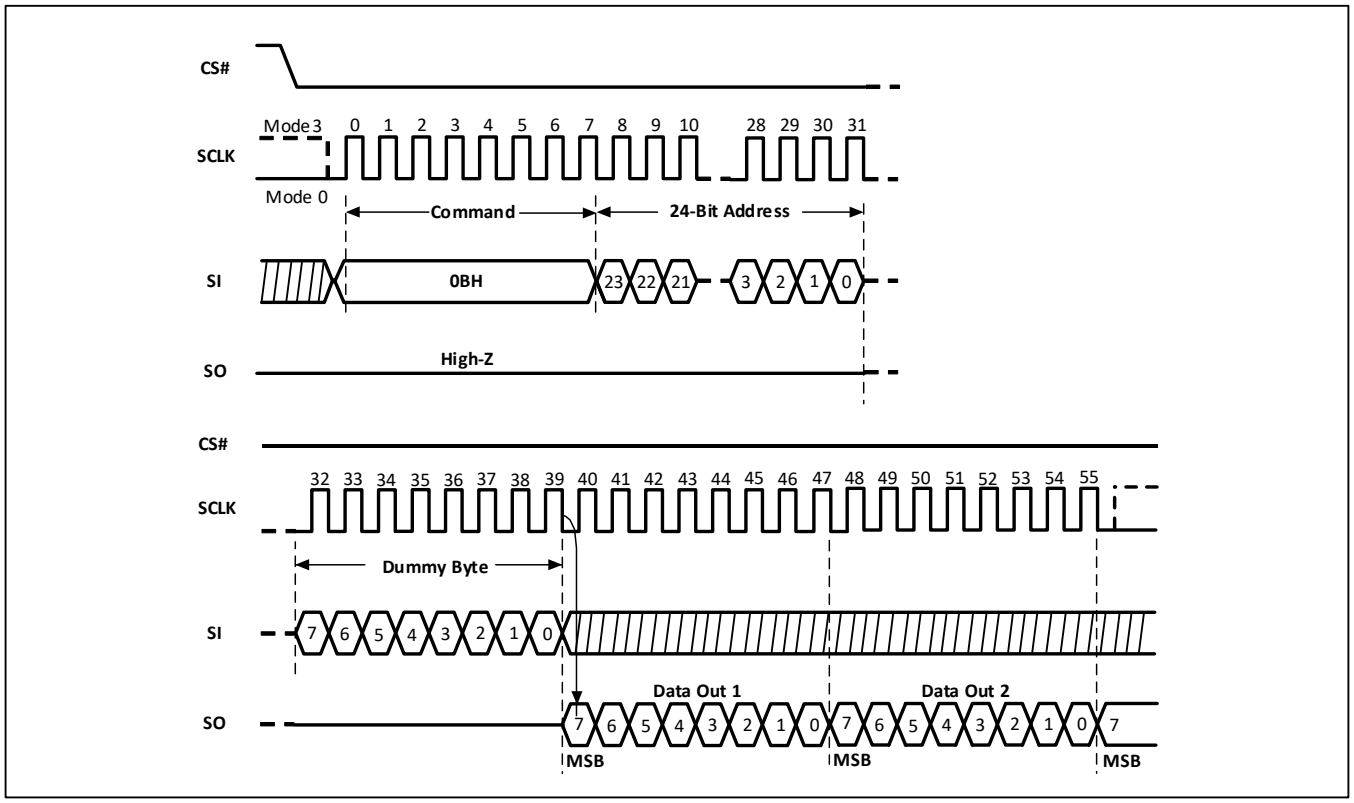
9.7 Read Data Bytes at Higher Speed (FAST_READ) (0BH)

The device is first selected by driving Chip Select (CS#) Low. The command code for the Read Data Bytes at Higher Speed (0BH) command is followed by a 3-byte address (A23-A0) and a dummy byte, each bit being latched-in on the rising edge of Serial Clock (SCLK). Then the memory contents, at that address, is shifted out on Data Output (SO), with each bit shifted out at a maximum frequency fC on the falling edge of SCLK.

The command sequence is shown in Figure-8. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The whole memory can, therefore, be read with a single FAST_READ command. When the highest address is reached, the address counter rolls over to 000000h, allowing the read sequence to be continued indefinitely.

The FAST_READ command is terminated by driving CS# High. CS# can be driven High at any time during data output. Any FAST_READ command, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure-8. Read Data Bytes at Higher Speed Sequence Diagram

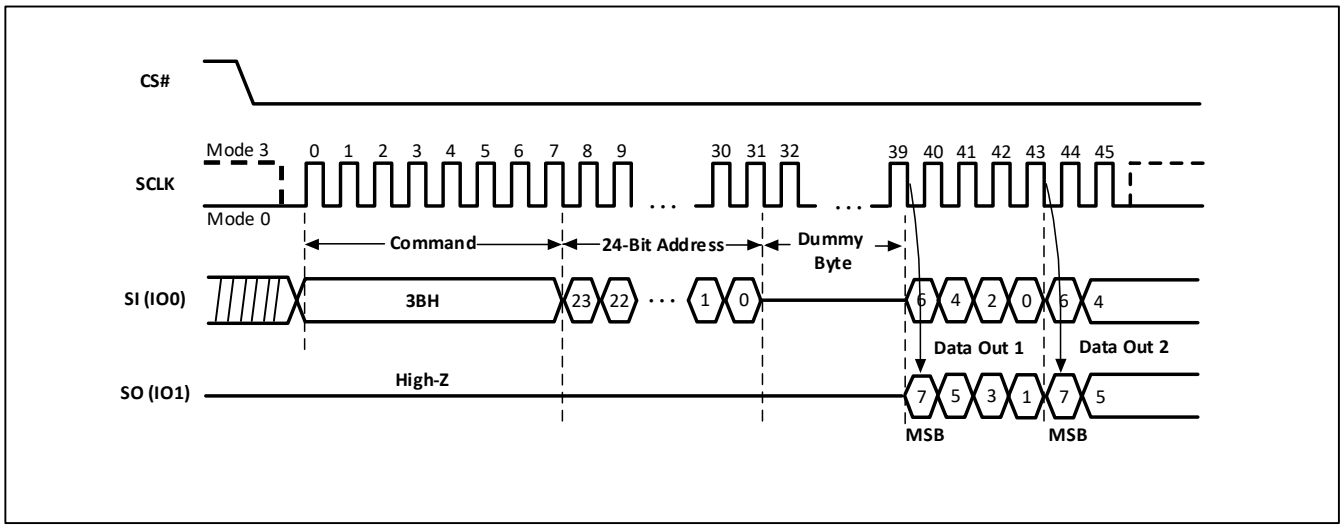


9.8 Dual Output Fast Read (DREAD) (3BH)

The Dual Output Fast Read (3BH) is similar to the standard Fast Read (0BH) command except that data is output on two pins, SI (IO0) and SO (IO1), instead of just SO. This allows data to be transferred from the UC25LDxx at twice the rate of standard SPI devices. The DREAD command is ideal for quickly downloading code from the flash to RAM upon power-up or for applications that cache code-segments to RAM for execution.

Like the Fast Read command, the DREAD command can operate at the highest possible frequency of fT. This is accomplished by adding eight “dummy clocks after the 24-bit address as shown in Figure-9. The dummy clocks allow the device’s internal circuits the time required for setting up the initial address. The input data during the dummy clock is “don’t care”. However, the SI pin should be in a high-impedance state prior to the falling edge of SLCK for the first data out.

Figure-9. Dual Output Fast Read Sequence Diagram



9.9 Page Erase (PE) (81H)

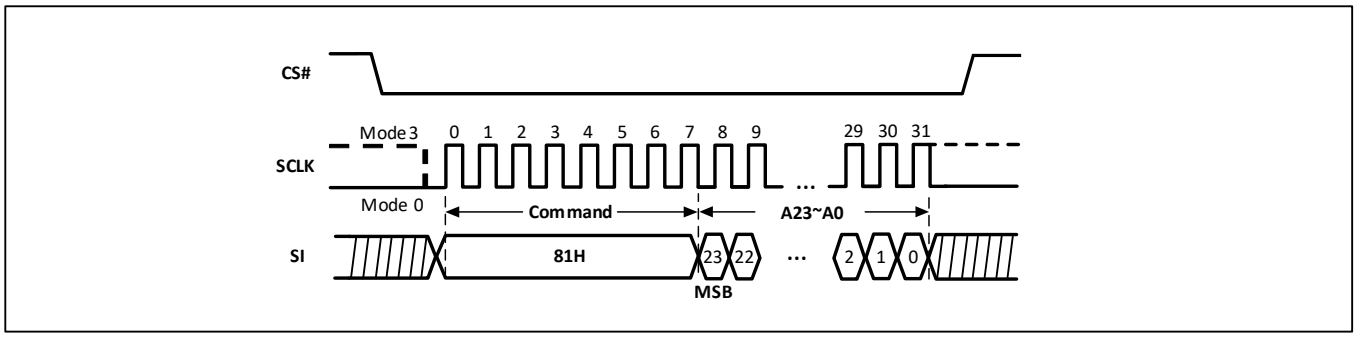
The Page Erase (81H) command sets all bits to 1 (FFh) inside the chosen page. Before it can be accepted, a Write Enable (06H) command must have previously been executed. After the Write Enable command has been decoded, the device sets the Write Enable Latch (WEL).

The PE command is entered by driving Chip Select (CS#) Low, followed by the command code, and three address bytes on Data Input (SI). Any address inside the page is a valid address for the PE command. CS# must be driven Low for the entire duration of the sequence.

The command sequence is shown in Figure-12. The CS# must go high exactly at the byte boundary (after the least significant bit of the third address byte is latched-in); otherwise, the command will be rejected and not executed. As soon as CS# is driven High, the self-timed Page Erase cycle (with duration tPE) is initiated. While the Page Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The WIP bit is 1 during the self-timed Page Erase cycle and is 0 when it is completed. At some unspecified time before the cycle is completed, the WEL bit is reset.

A PE command may be applied only to a page which is not protected by the Block Protect (BP2, BP1, BP0) bits.

Figure-12. Page Erase Sequence Diagram



9.10 Sector Erase (SE) (20H)

The Sector Erase (20H) command sets all bits to 1 (FFh) inside the chosen sector. Before it can be accepted, a Write Enable (06H) command must have previously been executed. After the Write Enable command has been decoded, the device sets the Write Enable Latch (WEL).

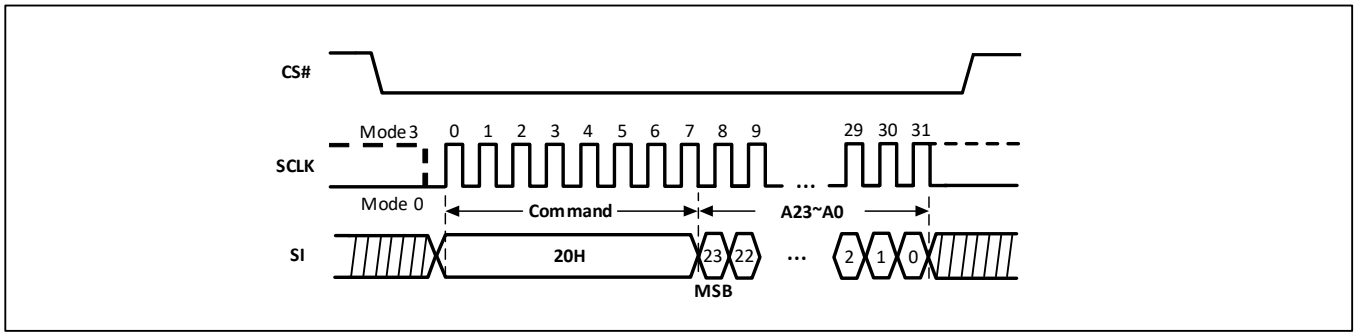
The SE command is entered by driving Chip Select (CS#) Low, followed by the command code, and

three address bytes on Data Input (SI). Any address inside the sector is a valid address for the SE command. CS# must be driven Low for the entire duration of the sequence.

The command sequence is shown in Figure-13. The CS# must go high exactly at the byte boundary (after the least significant bit of the third address byte is latched-in); otherwise, the command will be rejected and not executed. As soon as CS# is driven High, the self-timed Sector Erase cycle (with duration tSE) is initiated. While the Sector Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The WIP bit is 1 during the self-timed Sector Erase cycle and is 0 when it is completed. At some unspecified time before the cycle is completed, the WEL bit is reset.

A SE command may be applied only to a sector which is not protected by the Block Protect (BP2, BP1, BP0) bits.

Figure-13. Sector Erase Sequence Diagram



9.11 Half Block Erase (HBE) (52H)

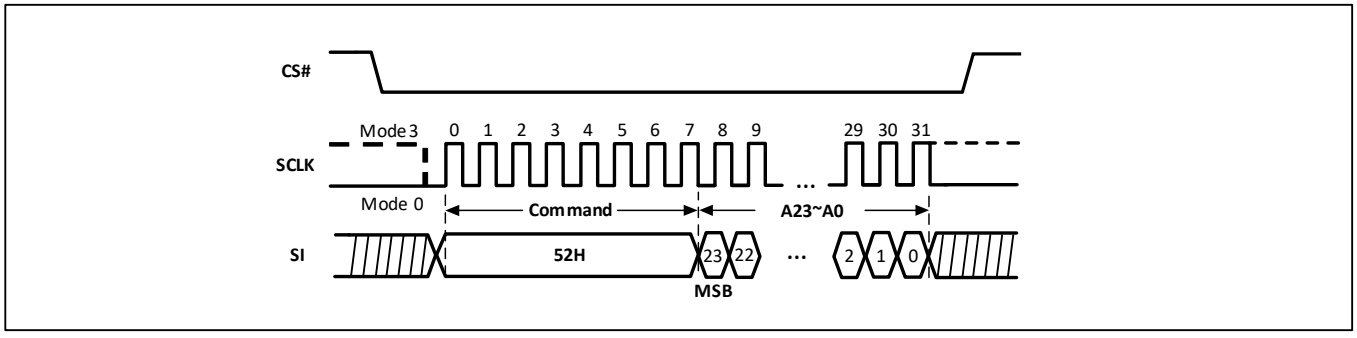
The Half Block Erase (52H) command sets all bits to 1 (FFh) inside the chosen block. Before it can be accepted, a Write Enable (06H) command must have previously been executed. After the Write Enable command has been decoded, the device sets the Write Enable Latch (WEL).

The HBE command is entered by driving Chip Select (CS#) Low, followed by the command code, and three address bytes on Data Input (SI). Any address inside the block is a valid address for the HBE command. CS# must be driven Low for the entire duration of the sequence.

The command sequence is shown in Figure-14. The CS# must go high exactly at the byte boundary (after the least significant bit of the third address byte is latched-in); otherwise, the command will be rejected and not executed. As soon as CS# is driven High, the self-timed Half Block Erase cycle (with duration tBE1) is initiated. While the Half Block Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The WIP bit is 1 during the self-timed Block Erase cycle and is 0 when it is completed. At some unspecified time before the cycle is completed, the WEL bit is reset.

A HBE command may be applied only to a half block which is not protected by the Block Protect (BP2, BP1, BP0) bits.

Figure-14. Half Block Erase Sequence Diagram



9.12 Block Erase (BE) (D8H)

The Block Erase (D8H) command sets all bits to 1 (FFh) inside the chosen block. Before it can be

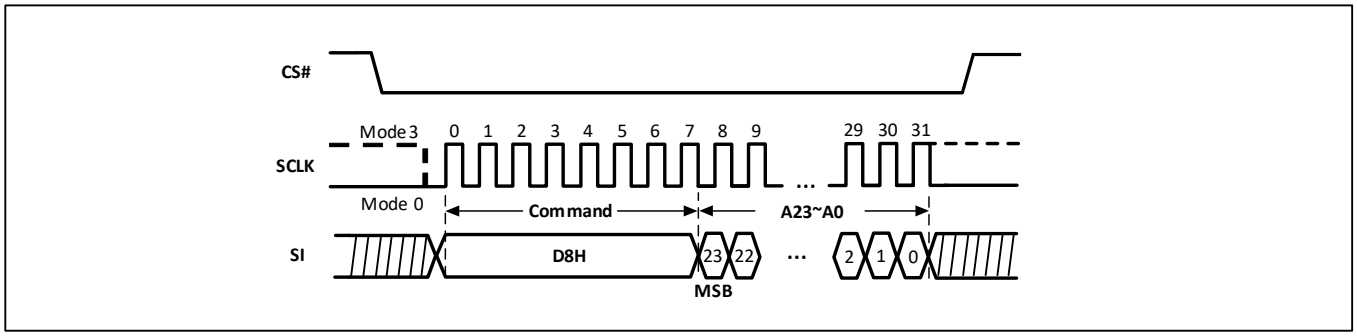
accepted, a Write Enable (06H) command must have previously been executed. After the Write Enable 06H command has been decoded, the device sets the Write Enable Latch (WEL).

The BE command is entered by driving Chip Select (CS#) Low, followed by the command code, and three address bytes on Data Input (SI). Any address inside the block is a valid address for the BE command. CS# must be driven Low for the entire duration of the sequence.

The command sequence is shown in Figure-15. CS# must be driven High after the least significant bit of the third address byte is latched in, otherwise the BE command is not executed. As soon as CS# is driven High, the self-timed Block Erase cycle (whose duration is tBE2) is initiated. While the Block Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The WIP bit is 1 during the self-timed Block Erase cycle and is 0 when it is completed. At some unspecified time before the cycle is completed, the WEL bit is reset.

A BE command may be applied only to a block which is not protected by the Block Protect (BP2, BP1, BP0) bits.

Figure-15. Block Erase Sequence Diagram



9.13 Chip Erase (CE) (60H or C7H)

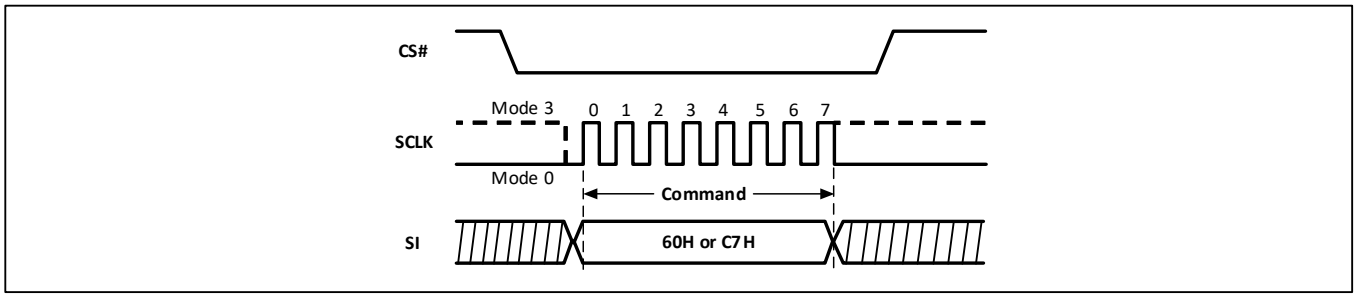
The Chip Erase (60H or C7H) command sets all bits to 1 (FFh). Before it can be accepted, a Write Enable (06H) command must have previously been executed. After the Write Enable command has been decoded, the device sets the Write Enable Latch (WEL).

The CE command is entered by driving Chip Select (CS#) Low, followed by the command code on Data Input (SI). CS# must be driven Low for the entire duration of the sequence.

The command sequence is shown in Figure-16. CS# must be driven High after the eighth bit of the command code is latched in, otherwise the CE command is not executed. As soon as CS# is driven High, the self-timed Chip Erase cycle (with duration tCE) is initiated. While the Chip Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The WIP bit is 1 during the self-timed Chip Erase cycle and is 0 when it is completed. At some unspecified time before the cycle is completed, the WEL bit is reset.

The CE command is executed only if all Block Protect (BP2, BP1, BP0) bits are 0. The CE command is ignored if one, or more blocks are protected.

Figure-16. Chip Erase Sequence Diagram



9.14 Page Program (PP) (02H)

The Page Program (02H) command allows bytes to be programmed in the memory. Before it can be accepted, a Write Enable (06H) command must have previously been executed. After the Write Enable command has been decoded, the device sets the Write Enable Latch (WEL).

The PP command is entered by driving Chip Select (CS#) Low, followed by the command code, three address bytes and at least one data byte on Data Input (SI). If the 8 least significant address bits (A7-A0) are not all zero, all transmitted data that goes beyond the end of the current page are programmed from the starting address of the same page (from the address whose 8 least significant bits (A7-A0) are all zero). CS# must be driven Low for the entire duration of the sequence.

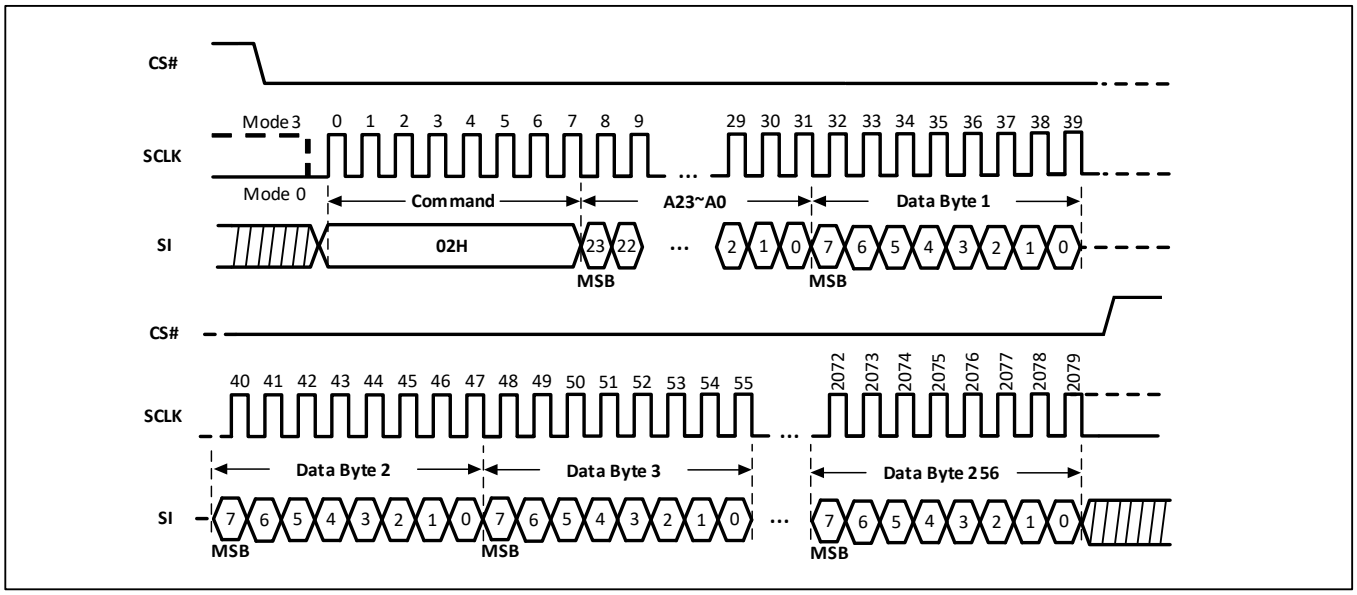
The command sequence is shown in Figure-17. If more than 256 bytes are sent to the device, previously latched data are discarded, and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 Data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page.

CS# must be driven High after the eighth bit of the last data byte has been latched in, otherwise the PP command is not executed.

As soon as CS# is driven High, the self-timed Page Program cycle (with duration tPP) is initiated. While the Page Program cycle is in progress, the Status Register may be read to check the value of the WIP bit. The WIP bit is 1 during the self-timed Page Program cycle and is 0 when it is completed. At some unspecified time before the cycle is completed, the WEL bit is reset.

A PP command may be applied only to a page which is not protected by the Block Protect (BP2, BP1, BP0) bits.

Figure-17. Page Program Sequence Diagram



9.15 Erase Security Register (ERSCUR) (44H)

There are two 256-byte Security Registers which can be erased and programmed individually. These registers may be used by system manufacturers to store security and other important information separately from the main memory array.

The Erase Security Register (44H) command is like the Sector Erase (20H) command. A Write Enable command must be executed before the device will accept the ERSCUR Command (Status Register bit WEL must equal 1). The command is initiated by driving the CS# pin low and shifting the command code “44H” followed by a 24-bit address (A23-A0) to erase one of the security registers.

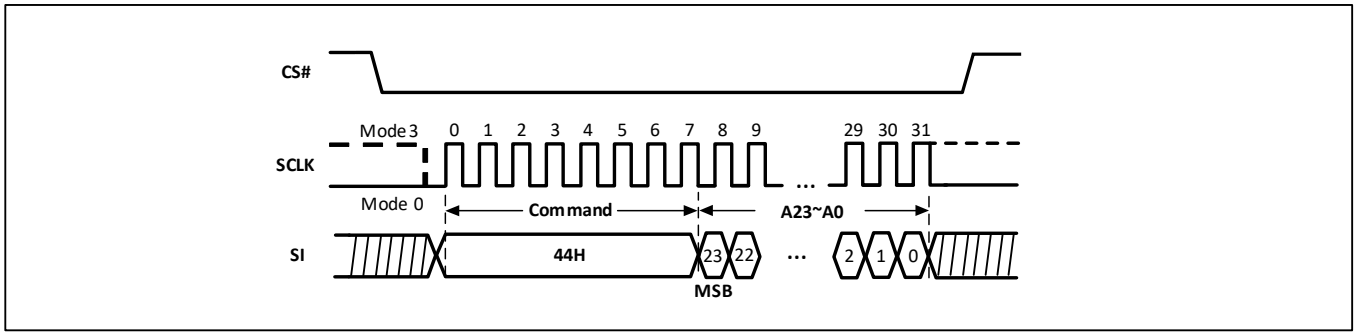
The ERSCUR command sequence is shown in Figure-18. The CS# pin must be driven high after the eighth bit of the last address byte is latched. If this is not done, the command will not be executed. After CS# is driven high, the self-timed ERSCUR operation will commence for a time duration of tSE.

While the Erase Security Register cycle is in progress, the Read Status Register command (05H) may still be accessed for checking the value of the Write in Progress (WIP) bit. The WIP bit is a 1 during the erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other commands again. After the Erase Security Register cycle has finished, the WEL bit in the Status Register is cleared to 0. The Security Register Lock Bits (LB1&LB2) in the Status Register are OTP and can be used to protect the security registers. Once the LB1&LB2 bit is set to 1, the corresponding security register will be permanently locked, and an ERSCUR command to that register will be ignored.

Table-8.0 Erase Security Register Address

ADDRESS	A23-16	A15-12	A11-8	A7-0
Security Register #1	00h	0001	0000	Don't care
Security Register #2	00h	0010	0000	Don't care

Figure-18. Erase Security Register Sequence Diagram



9.16 Program Security Register (PRSCUR) (42H)

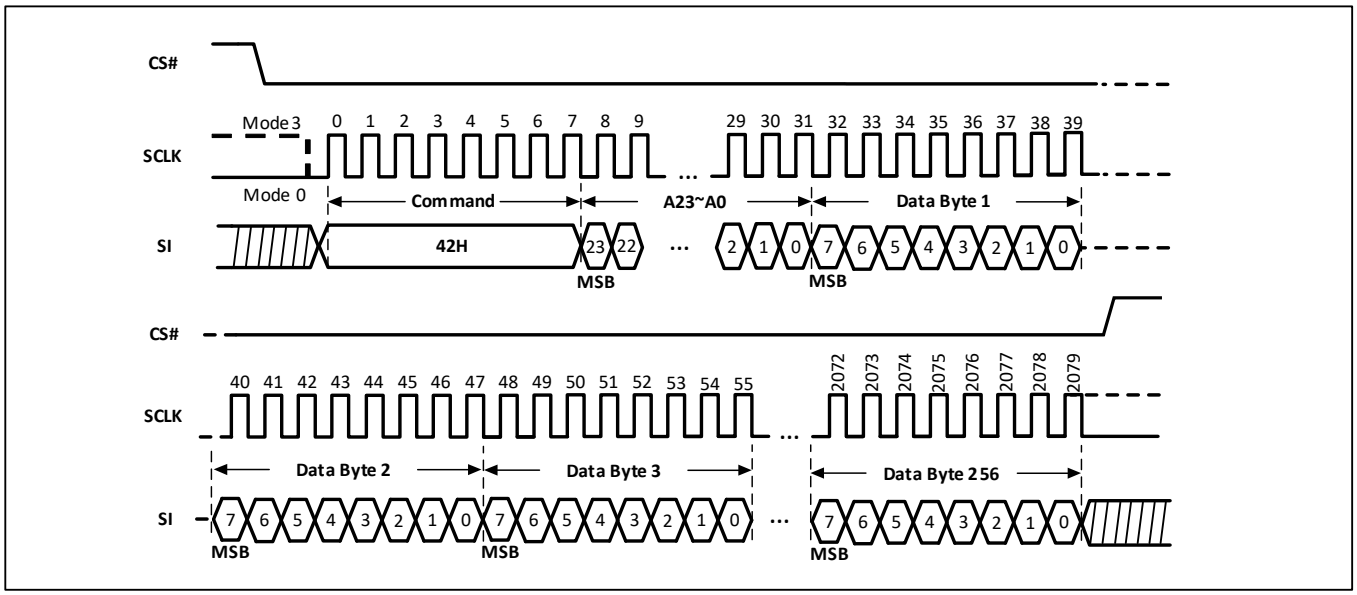
The Program Security Register (42H) command is similar to the Page Program (02H) command. It allows from one byte to 256 bytes of security register data to be programmed at previously erased (FFh) memory locations. A Write Enable (06H) command must be executed before the device will accept the PRSCUR Command (Status Register bit WEL= 1). The command is initiated by driving the CS# pin low then shifting the command code "42H" followed by a 24-bit address (A23-A0) and at least one data byte, into the SI pin. The CS# pin must be held low for the entire length of the command while data is being sent to the device.

The PRSCUR command sequence is shown in Figure-19. The Security Register Lock Bits (LB1&LB2) in the Status Register are OTP can be used to protect the security registers. Once Security Register Lock Bit (LB1&LB2) is set to 1, the corresponding security register will be permanently locked, and a PRSCUR command to that register will be ignored.

Table-8.1 Program Security Register Address

ADDRESS	A23-16	A15-12	A11-8	A7-0
Security Register #1	00h	0001	0000	Byte Address
Security Register #2	00h	0010	0000	Byte Address

Figure-19. Program Security Register Sequence Diagram



9.17 Read Security Register (RDSCUR) (48H)

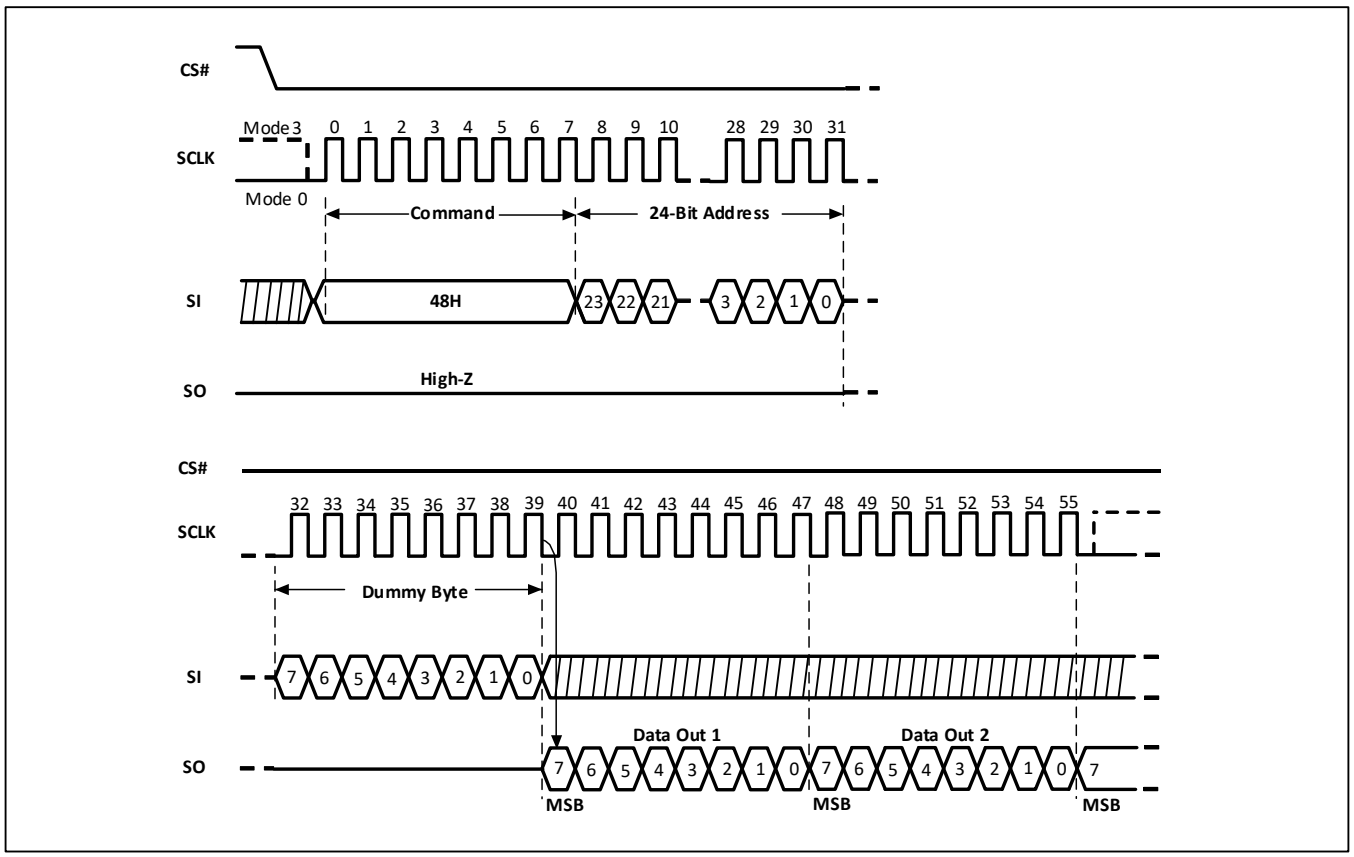
The Read Security Register (48H) command is similar to the Fast Read (0BH) command and allows one or more data bytes to be sequentially read from one of the three security registers. The command is initiated by driving the CS# pin low and then shifting the command code “48H” followed by a 24-bit address (A23-A0) and eight “dummy” clocks into the SI pin. The code and address bits are latched on the rising edge of the SCLK pin. After the address is received, and following the eight dummy cycles, the data byte of the addressed memory location will be shifted out on the SO pin on the falling edge of SCLK with the most significant bit (MSB) first. The first byte addressed can be at any location. The byte address is automatically incremented to the next byte address after each byte of data is shifted out. Once the byte address reaches the last byte of the register (byte FFh), it will reset to 00h, the first byte of the register, and continue to increment. The command is completed by driving CS# high.

The RDSCUR command sequence is shown in Figure-20. If a RDSCUR command is issued while an Erase, Program, or Write cycle is in process (Write in Progress (WIP)=1), the command is ignored and will not have any effect on the current cycle. The RDSCUR command allows each bit being shifted out on SO pin at a Max frequency fC, on the falling edge of SCLK.

Table-8.2 Read Security Register Address

ADDRESS	A23-16	A15-12	A11-8	A7-0
Security Register #1	00h	0001	0000	Byte Address
Security Register #2	00h	0010	0000	Byte Address

Figure-20. Read Security Register Sequence Diagram



9.18 Deep Power-Down (DP) (B9H)

Executing the Deep Power-Down (B9H) command is the only way to place the device in the lowest power consumption mode (the Deep Power-Down mode). It can also be used as an extra software protection mechanisms the device is not in active use, all Write, Program and Erase commands are ignored.

Driving Chip Select (CS#) High deselects the device and puts the device in the Standby mode (if there is no internal cycle currently in progress). However, Standby mode is not the Deep Power-Down mode. The Deep Power-Down mode can only be entered by executing the DP command, to reduce the standby current (from ISB1 to ISB2).

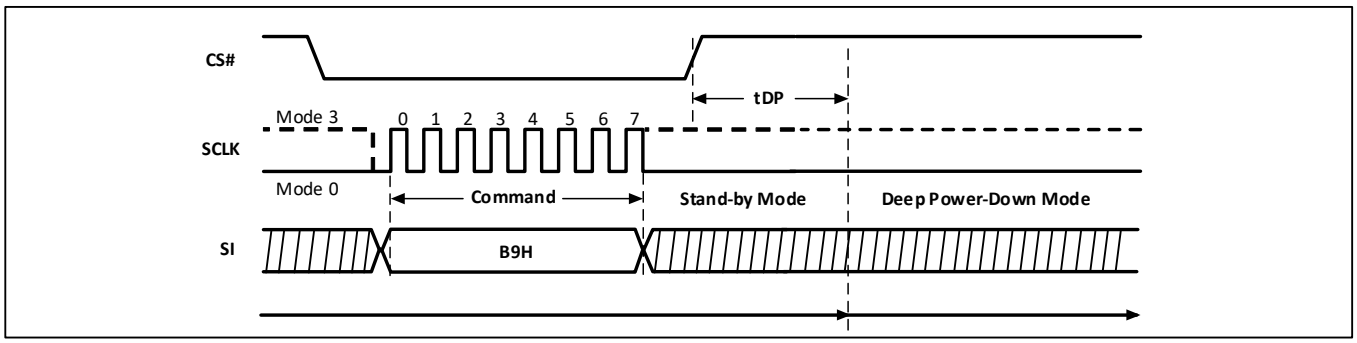
Once the device has entered the Deep Power-Down mode, all commands are ignored except the Release from Deep Power-Down, Read Electronic Signature (ABH) command. This command releases the device from this mode and also outputs the Device ID on Data Output (SO).

The Deep Power-Down mode automatically stops at Power-Down, and the device always Powers-up in the Standby mode. The DP command is entered by driving CS# Low, followed by the command code on Data Input (SI). CS# must be driven Low for the entire duration of the sequence.

The command sequence is shown in Figure-21. CS# must be driven High after the eighth bit of the command code has been latched in, otherwise the Deep Power-Down (B9H) command is not executed. As soon as CS# is driven High, a delay of tDP occurs before the supply current is reduced to ISB2 and the Deep Power-Down mode is entered.

Any DP command, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure-21. Deep Power-Down Sequence Diagram



9.19 Release form Deep Power-Down (RDP), Read Electronic Signature (RES) (ABH)

Once the device has entered the Deep Power-Down mode, all commands are ignored except the Release from Deep Power-Down, Read Electronic Signature (ABH) command. Executing this command takes the device out of the Deep Power-Down mode.

Please note that this is not the same as or even a subset of, the JEDEC 16-bit Electronic Signature that is read by the Read Identification (9FH) command. The old-style Electronic Signature is supported for reasons of backward compatibility, only, and should not be used for new designs. New designs should, instead, make use of the JEDEC 16-bit Electronic Signature, and the Read Identification command.

When used only to release the device from the power-down state, the command is issued by driving the Chip Select (CS#) pin low, shifting the command code “ABH” and driving CS# high as shown in Figure-22. After the time duration of tRES1 the device will resume normal operation and other commands will be accepted. The CS# pin must remain high during the tRES1 time duration.

When used only to obtain the Device ID while not in the power-down state, the command is initiated by driving the CS# pin low and shifting the command code “ABH” followed by 3-dummy bytes. The Device ID bits are then shifted out on the falling edge of SCLK with the most significant bit (MSB) first as shown in Figure-23. The Device ID values are listed in "Tables of ID Definition" (Table-7.X). The Device ID can be read continuously. The command is completed by driving CS# high.

When CS# is driven High, the device is put in the Stand-by Power mode. If the device was not previously in the Deep Power-Down mode, the transition to the Stand-by Power mode is immediate. If the device was previously in the Deep Power-Down mode, though, the transition to the Stand-by Power mode is delayed by tRES2, and CS# must remain High for at least tRES2 (max). Once in the Stand-by Power mode, the device waits to be selected, so that it can receive, decode and execute commands.

Except while an Erase, Program or Write Status Register cycle is in progress, the RDP, RES command always provides access to the 8-bit Device ID of the device and can be applied even if the Deep Power-Down mode has not been entered.

Any RDP, RES command issued to the device while an Erase, Program or Write Status Register cycle is in progress, is not decoded, and has no effect on the cycle that is in progress.

Figure-22. Release from Deep Power-Down (RDP) Sequence Diagram

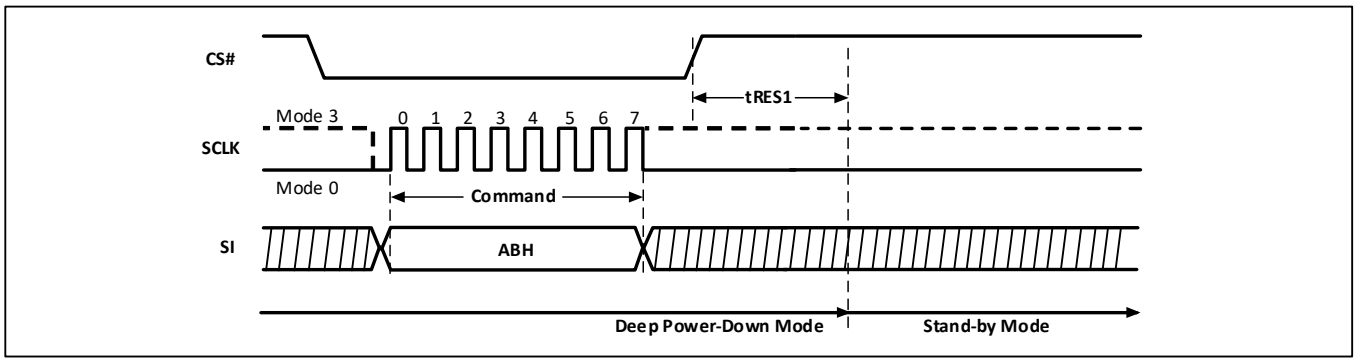
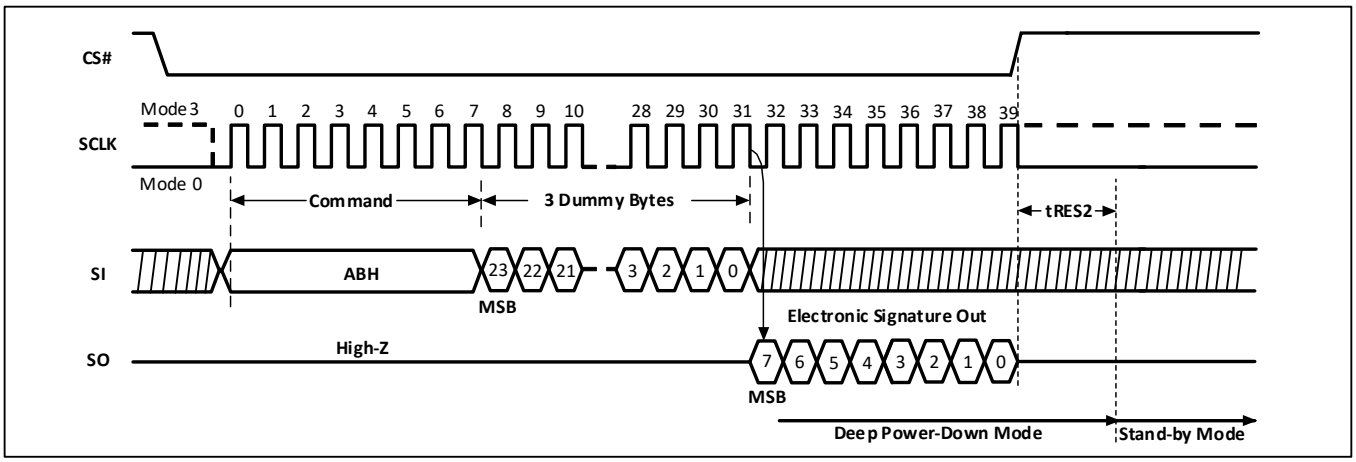


Figure-23. Read Electronic Signature (RES) Sequence Diagram

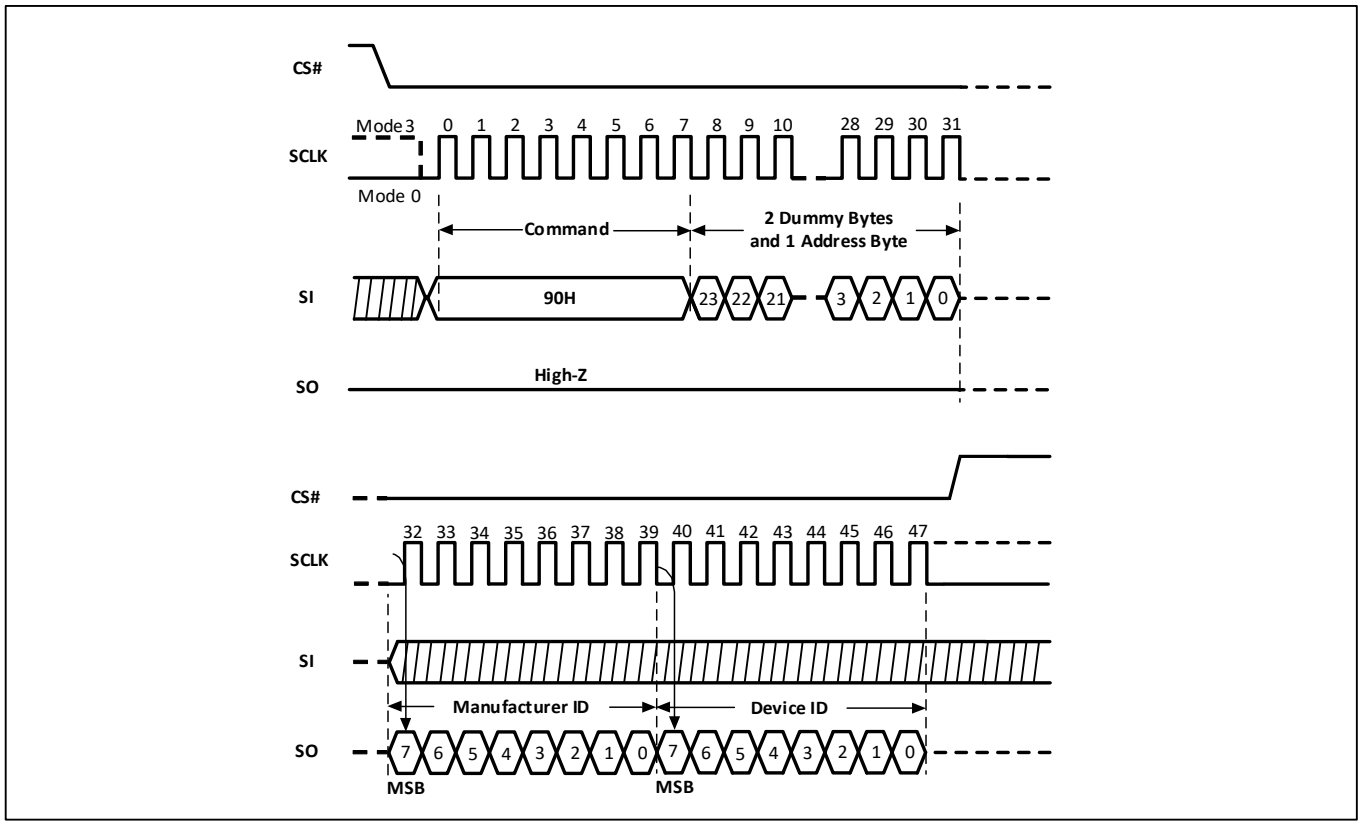


9.20 Read Electronic Manufacturer ID & Device ID (REMS) (90H)

The Read Electronic Manufacturer & Device ID (90H) command provides both the JEDEC assigned Manufacturer ID and the specific Device ID.

The REMS command is initiated by driving the CS# pin low and shifting the command code “90H” followed by two dummy bytes and one address byte (A7~A0). After which, the Manufacturer ID for UCUN (B3h) and the Device ID are shifted out on the falling edge of SCLK with the most significant bit (MSB) first as shown in Figure-24. The Device ID values are listed in "Tables of ID Definition" (Table-7.X). If the address byte is 00h, the manufacturer ID will be output first, followed by the device ID. If the address byte is 01h, then the device ID will be output first, followed by the manufacturer ID. While CS# is low, the Manufacturer and Device IDs can be read continuously, alternating from one to the other. The command is completed by driving CS# high.

Figure-24. Read Electronic Manufacturer ID & Device ID Sequence Diagram



9.21 Read Identification (RDID) (9FH)

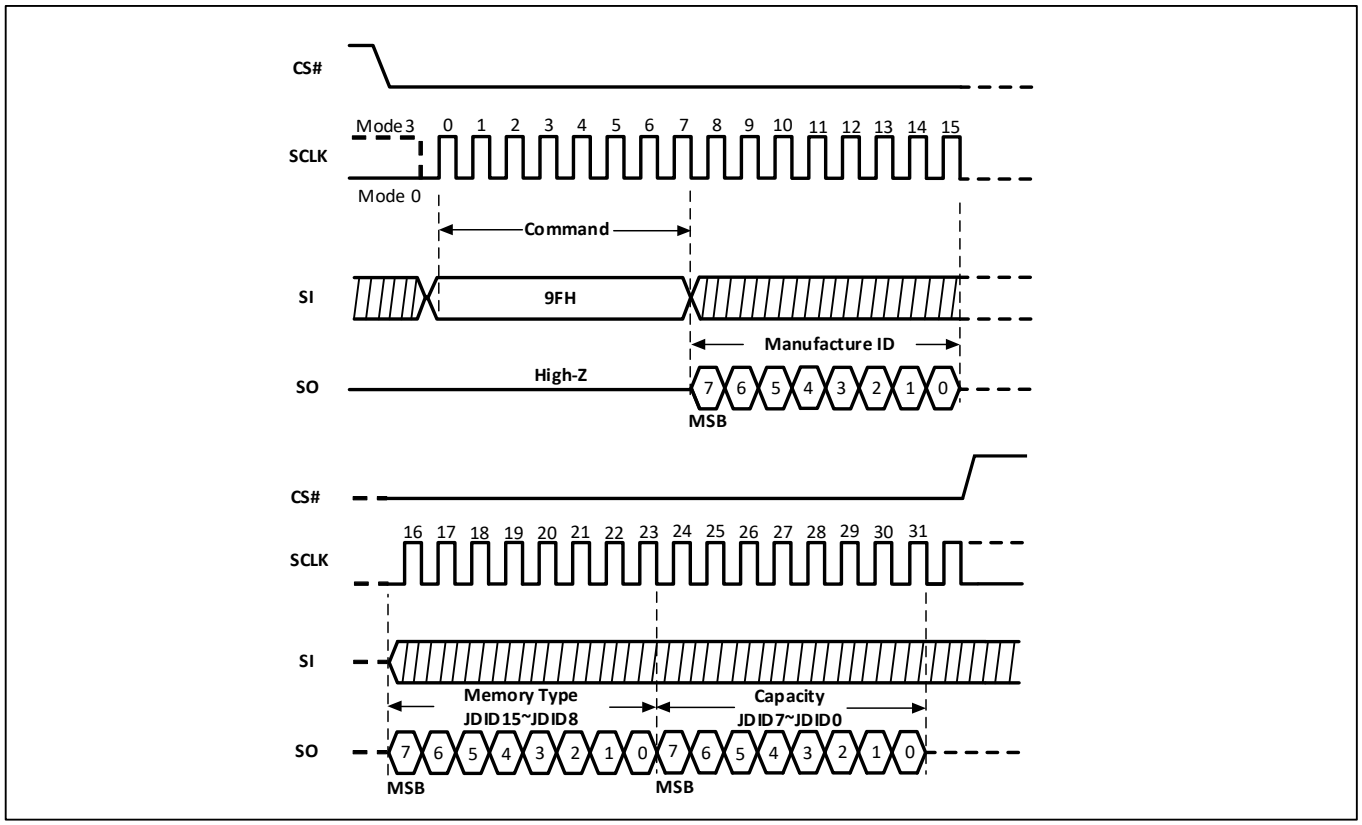
The Read Identification (9FH) command allows the 8-bit Manufacturer ID to be read, followed by two bytes of Device ID. The Device ID indicates the memory type in the first byte, and the memory capacity of the device in the second byte. The UCUN Manufacturer ID and Device ID are list as "Tables of ID Definition" (Table-7.X).

Any RDID command issued while an Erase or Program cycle is in progress, is not decoded, and has no effect on the cycle that is in progress. The RDID command should not be issued while the device is in Deep Power down mode.

The device is first selected by driving the CS# Low. Then the 8-bit command code for the command is shifted in. This is followed by the 24-bit device identification stored in the memory, shifted out on the SO pin on the falling edge of SCLK. The command sequence is shown in Figure-26. The RDID command is terminated by driving CS# High at any time during data output.

When CS# is driven High, the device is placed in the standby mode. Once in the standby stage, the device waits to be selected, so that it can receive, decode and execute commands.

Figure-26. Read Identification Sequence Diagram

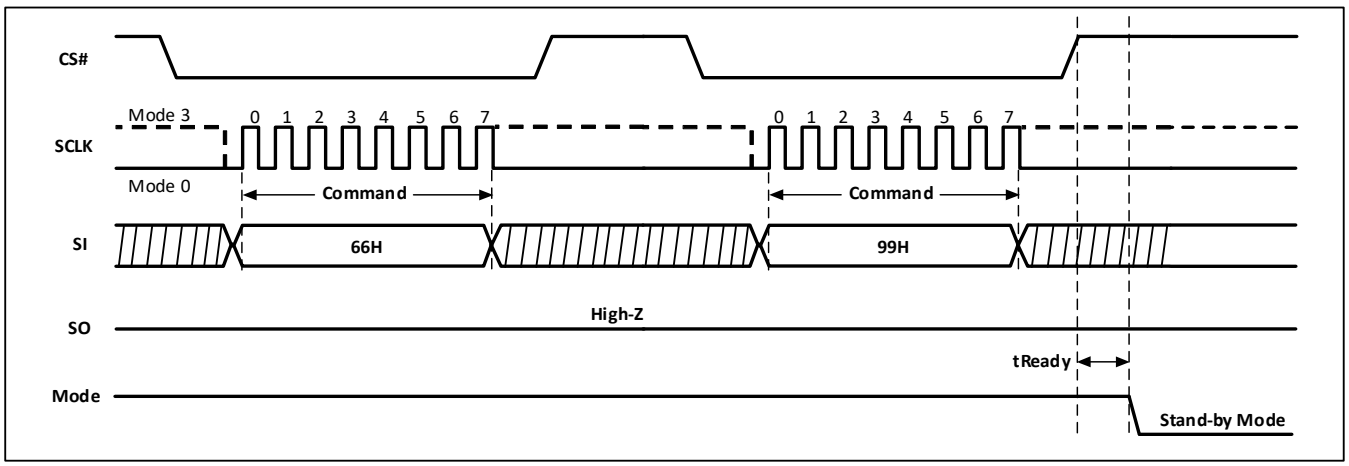


9.22 Reset Enable (RSTEN) (66H) and Reset (RST) (99H)

The Software Reset operation combines two commands: Reset Enable (66H) command and Reset (99H) command. It returns the device to standby mode. All the volatile bits and settings will be cleared which returns the device to the same default status as power on. The Reset command immediately following a Reset Enable command, initiates the Software Reset process. Any command other than Reset following the Reset Enable command, will clear the reset enable condition and prevent a later Reset command from being recognized.

If the Reset command is executed during a program or erase operation, the operation will be disabled and the data under processing could be damaged or lost.

Figure-27. Reset Enable and Reset Sequence Diagram

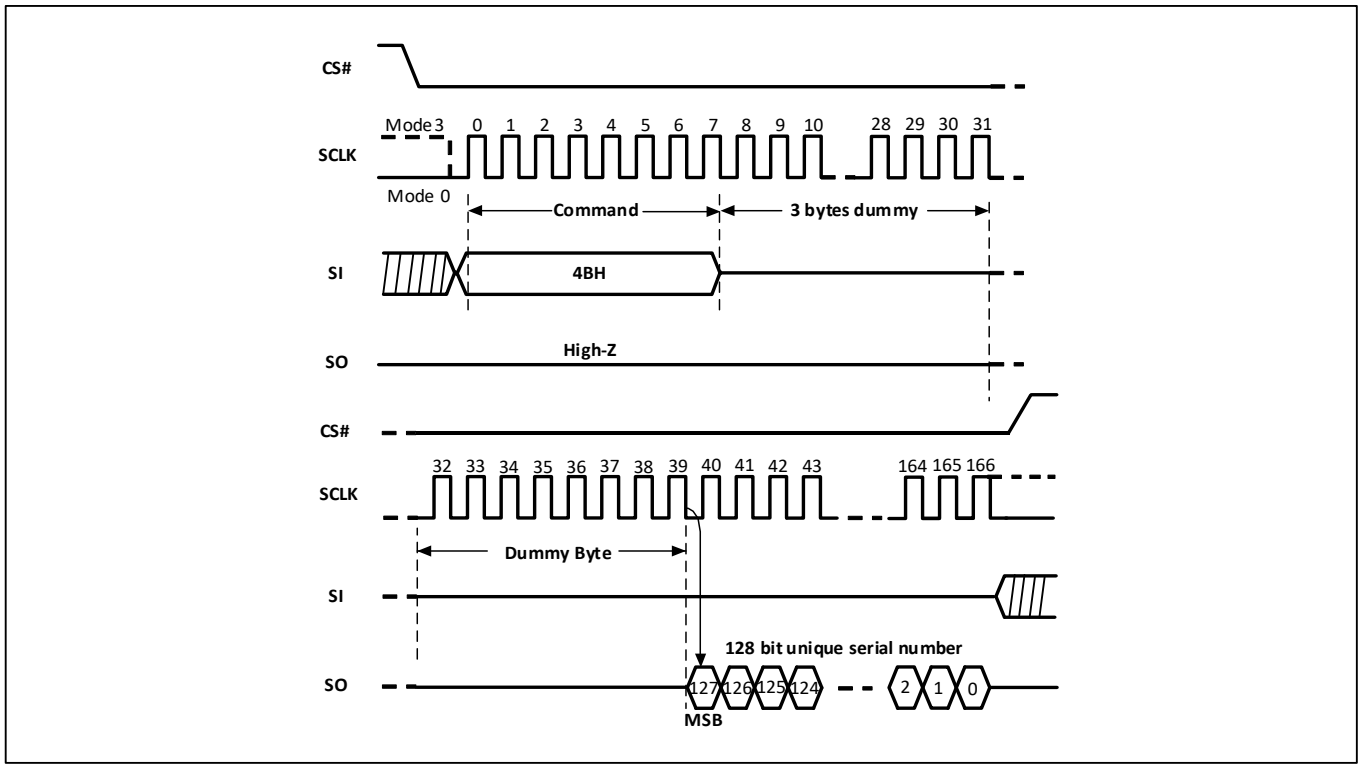


9.23 Read Unique ID (RUID) (4BH)

The Read Unique ID (4BH) command accesses a factory-set read-only 128-bits number that is unique to each UC25LDxx device. The ID number can be used in conjunction with user software methods to help prevent copying or cloning of a system.

The RUID command is initiated by driving the CS# pin low and shifting the command code “4BH” followed by four dummy bytes. Then, the 128-bits ID is shifted out on the falling edge of SCLK as shown in Figure-28.

Figure-28. Read Unique ID Sequence Diagram



10. ELECTRICAL SPECIFICATIONS

10.1 POWER-ON TIMING

Figure-29. Power-On Timing Sequence Diagram

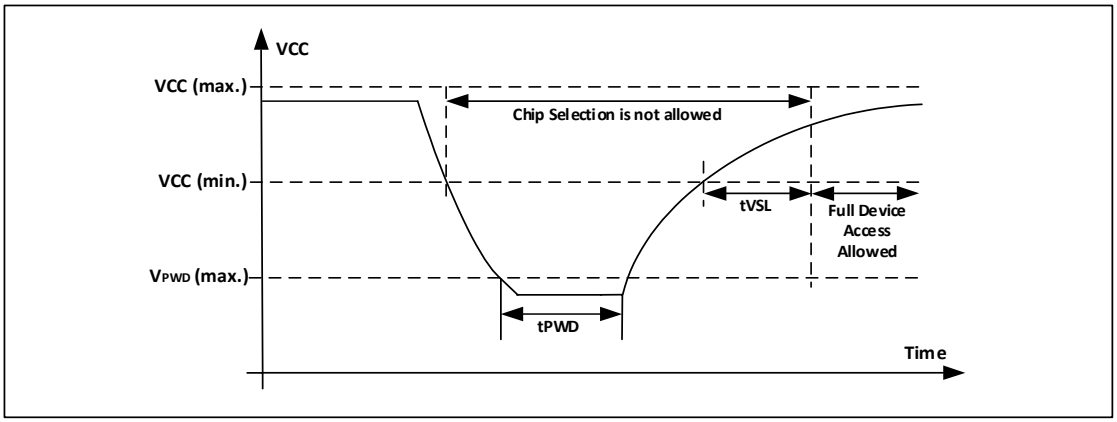


Table-9 Power-Up Timing and Write Inhibit Threshold

Sym.	Parameter	Min.	Max.	Unit
tVSL	VCC(min.) to device operation	0.3		ms
VWI	Write Inhibit Voltage	1	1.55	V
VPWD	VCC voltage needed to below VPWD for ensuring initializtion will occur		0.5	V
tPWD	The minimum duration for ensuring initialization will occur	300		us

10.2 INITIAL DELIVERY STATE

The device is delivered with the memory array erased: all bits are set to 1(each byte contains FFH).The Status Register contains 00H (all Status Register bits are 0).

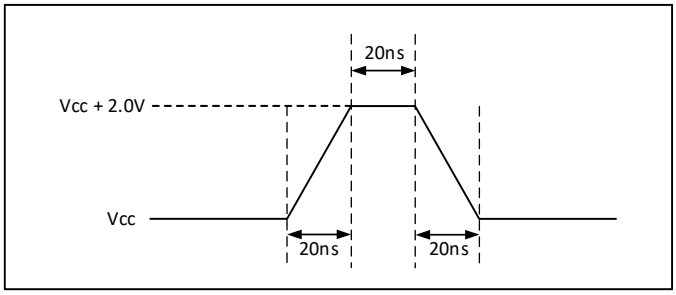
10.3 ABSOLUTE MAXIMUM RATINGS

Table-10 Absolute Maximum Ratings

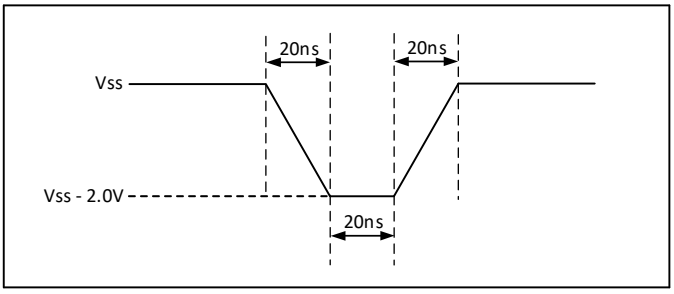
Parameter	Value	Unit
Ambient Operating Temperature	-40 to 85	°C
Storage Temperature	-65 to 150	°C
Applied Input / Output Voltage	-0.6 to VCC+0.4	V
Transient Input / Output Voltage(note: overshoot)	-2.0 to VCC+2.0	V
VCC	-0.6 to 4.2	V

Figure-30. Maximum Negative/positive Overshoot Diagram

Maximum Negative Overshoot Waveform



Maximum Positive Overshoot Waveform



10.4 AC MEASUREMENT CONDITIONS

Table-11. AC Measurement Conditions

Sym.	Parameter	Min.	Typ.	Max	Unit	Conditions
CIN	Input Capacitance			6	pF	VIN = 0V
COUT	Output Capacitance			8	pF	VOUT = 0V
CL	Load Capacitance		30		pF	
	Input			5	ns	
	Input Pulse Voltage		0.1VCC to 0.8VCC		V	
	Input Timing Reference Voltage		0.2VCC to 0.7VCC		V	
	Output Timing Reference Voltage		0.5VCC			

10.5 DC CHARACTERISTICS

Table-12. DC Parameters (Ta=-40°C to +85°C)

Symbol	Parameter	Conditions	1.65V to 2.0V			Units
			Min.	Typ.	Max.	
I_{DPD}	Deep power down current	CS#=Vcc, all other inputs at 0V or Vcc		0.5	1.0	uA
I_{SB}	Standby current	CS#, HOLD#, WP#=Vcc all inputs at CMOS levels		0.5	1.0	uA
I_{CC1}	Low power read current (03h)	f=1MHz; IOUT=0mA		1.0	1.5	mA
		f=33MHz; IOUT=0mA		1.5	2.0	mA
I_{CC2}	Read current (0Bh)	f=50MHz; IOUT=0mA		1.8	2.5	mA
I_{CC3}	Program current	CS#=Vcc		3.0	4.0	mA
I_{CC4}	Erase current	CS#=Vcc		3.0	4.0	mA
I_{LI}	Input load current	All inputs at CMOS level			1.0	uA
I_{LO}	Output leakage	All inputs at CMOS level			1.0	uA
V_{IL}	Input low voltage				0.2Vcc	V
V_{IH}	Input high voltage		0.8Vcc			V
V_{OL}	Output low voltage	IOL=100uA			0.2	V
V_{OH}	Output high voltage	IOH=-100uA	Vcc-0.2			V

Note:

1.Typical values measured at 1.8V @ 25°C for the 1.65V to 2.0V range.

10.6 AC CHARACTERISTICS

Table-13. AC Parameters (Ta=-40°C to +85°C)

Symbol	Alt.	Parameter	1.65V~2.0V			Unit
			min.	typ	max.	
fsclk	fC	Clock Frequency for the following instructions: FAST_READ, PP, SE, BE32K, BE, CE, DP,RES, WREN, WRDI, RDID, RDSR, WRSR(4)			80	MHz
fRSCLK	fR	Clock Frequency for READ instructions			50	MHz
fTSCLK	fT	Clock Frequency for DREAD instructions			65	MHz
tCH(1)	tCLH	Clock High Time	5.5			ns
tCL(1)	tCLL	Clock Low Time (fSCLK) 45% x (1fSCLK)	5.5			ns
tCLCH(4)		Clock Rise Time (peak to peak)	0.1			v/ns
tCHCL(4)		Clock Fall Time (peak to peak)	0.1			v/ns
tSLCH	tCSS	CS# Active Setup Time (relative to SCLK)	5			ns
tCHSL		CS# Not Active Hold Time (relative to SCLK)	5			ns
tDVCH	tDSU	Data In Setup Time	2			ns
tCHDX	tDH	Data In Hold Time	3			ns
tCHSH		CS# Active Hold Time (relative to SCLK)	5			ns
tSHCH		CS# Not Active Setup Time (relative to SCLK)	5			ns
tSHSL	tCSH	CS# Deselect Time From Read to next Read	20			ns
		CS# Deselect Time From Write,Erase,Program to Read Status Register	30			ns
		Volatile Status Register Write Time	40			ns
tSHQZ(4)	tDIS	Output Disable Time			6	ns
tCLQV	tV	Clock Low to Output Valid Loading 30pF			12	ns
		Clock Low to Output Valid Loading 15pF			10	ns
tCLQX	tHO	Output Hold Time	0			ns
tHLCH		HOLD# Active Setup Time (relative to SCLK)	5			ns
tCHHH		HOLD# Active Hold Time (relative to SCLK)	5			ns
tHHCH		HOLD# Not Active Setup Time (relative to SCLK)	5			ns
tCHHL		HOLD# Not Active Hold Time (relative to SCLK)	5			ns
tHHQX	tLZ	HOLD# to Output Low-Z			6	ns
tHLQZ	tHZ	HOLD# to Output High-Z			6	ns
tWHSL(3)		Write Protect Setup Time	20			ns
tSHWL(3)		Write Protect Hold Time	100			ns
tDP		CS# High to Deep Power-down Mode			3	us
tRES1		CS# High To Standby Mode Without Electronic Signature Read			8	us
tRES2		CS# High To Standby Mode With Electronic Signature Read			8	us
tW		Write Status Register Cycle Time		8	12	ms
tReady		Reset recovery time(for erase/program operation except WRSR)	50			us
		Reset recovery time(for WRSR operation)		8	13	ms

Table-14. AC Parameters for Program and Erase (Ta=-40°C to +85°C)

Sym.	Parameter	1.65V to 2.0V			Units
		Min.	Typ.	Max.	
t_{PP}	Page program time (up to 256 bytes)		2	3	ms
t_{PE}	Page erase time		15	20	ms
t_{SE}	Sector erase time		15	20	ms
t_{BE1}	Block erase time for 32K bytes		15	20	ms
t_{BE2}	Block erase time for 64K bytes		15	20	ms
t_{CE}	Chip erase time		15	20	ms

Notes:

1. tCH + tCLmust be greater than or equal to 1/Frequency.
2. Typical values given for TA=25°C. Not 100% tested.
3. Only applicable as a constraint for a WRSR command.
4. The value guaranteed by characterization, not 100% tested in production.

Figure-31. Serial Input Timing

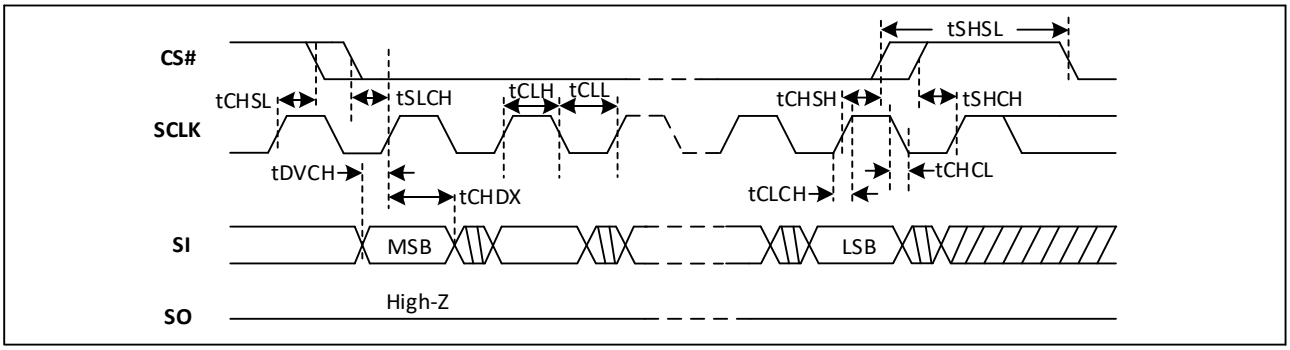


Figure-32. Output Timing

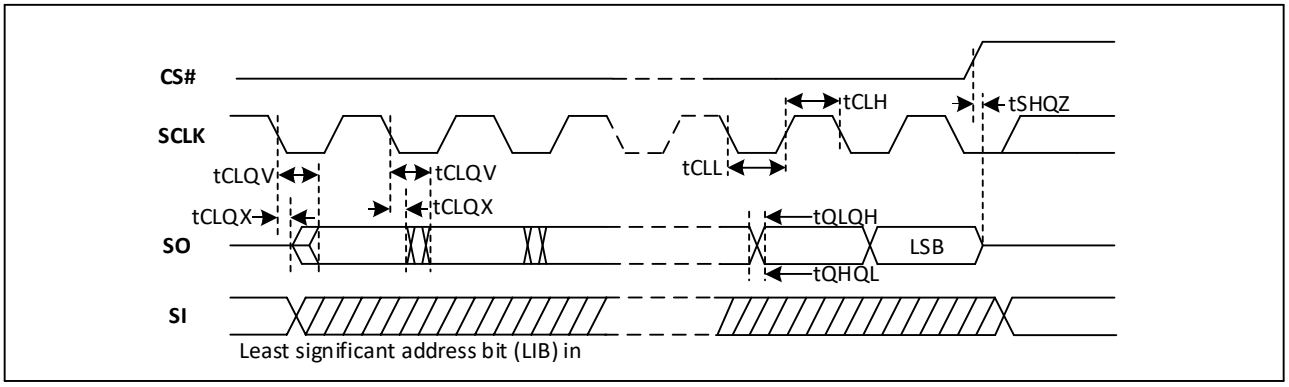
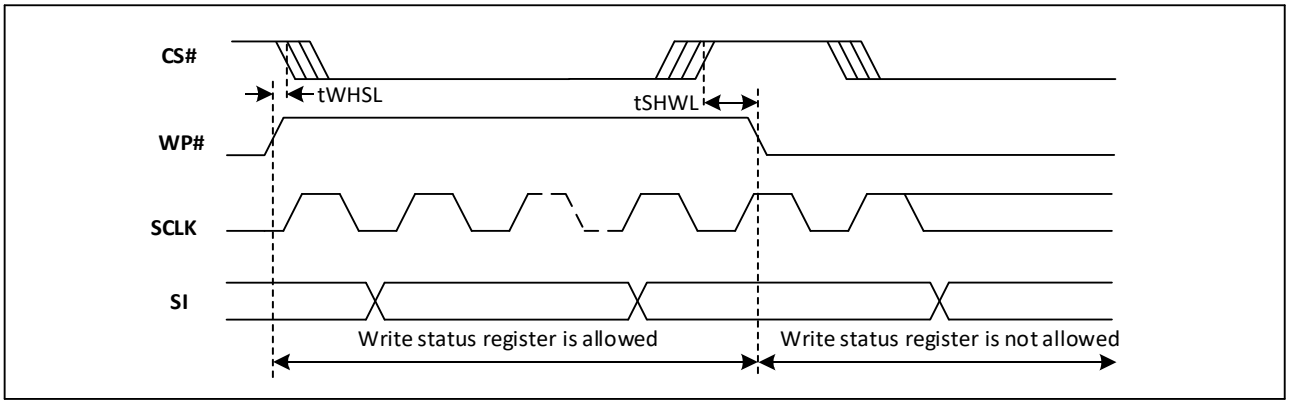
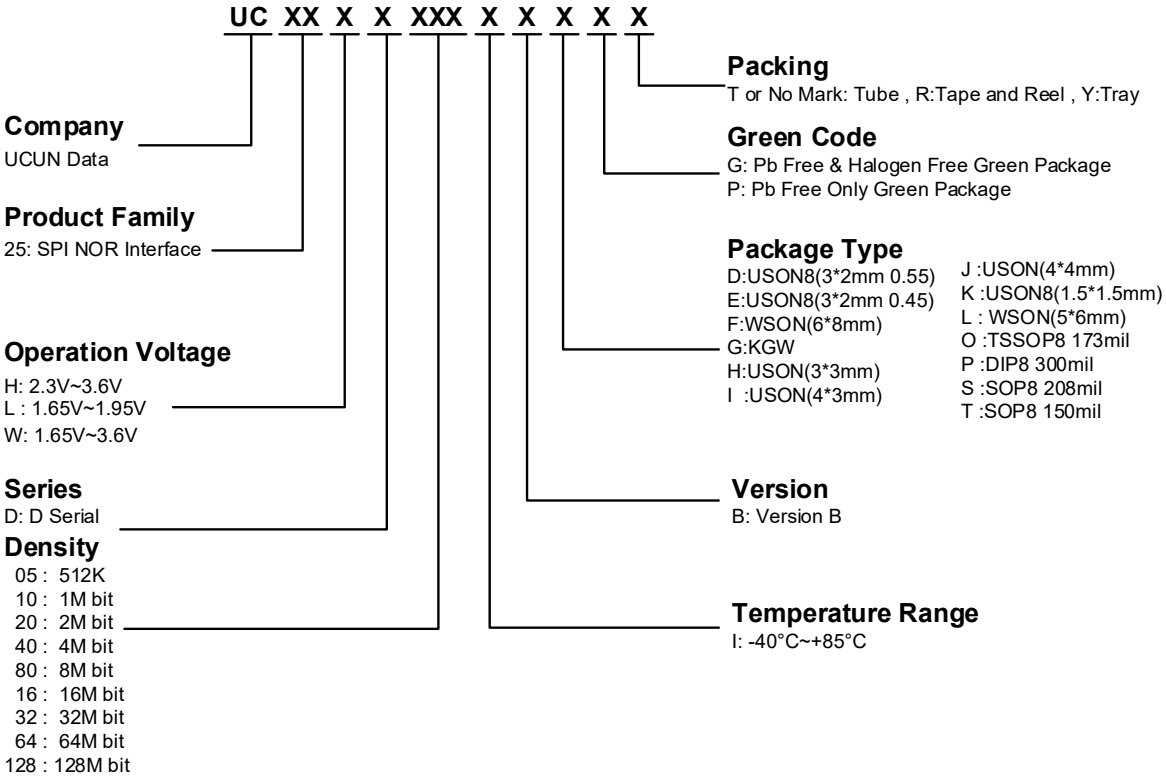


Figure-33. WP Timing

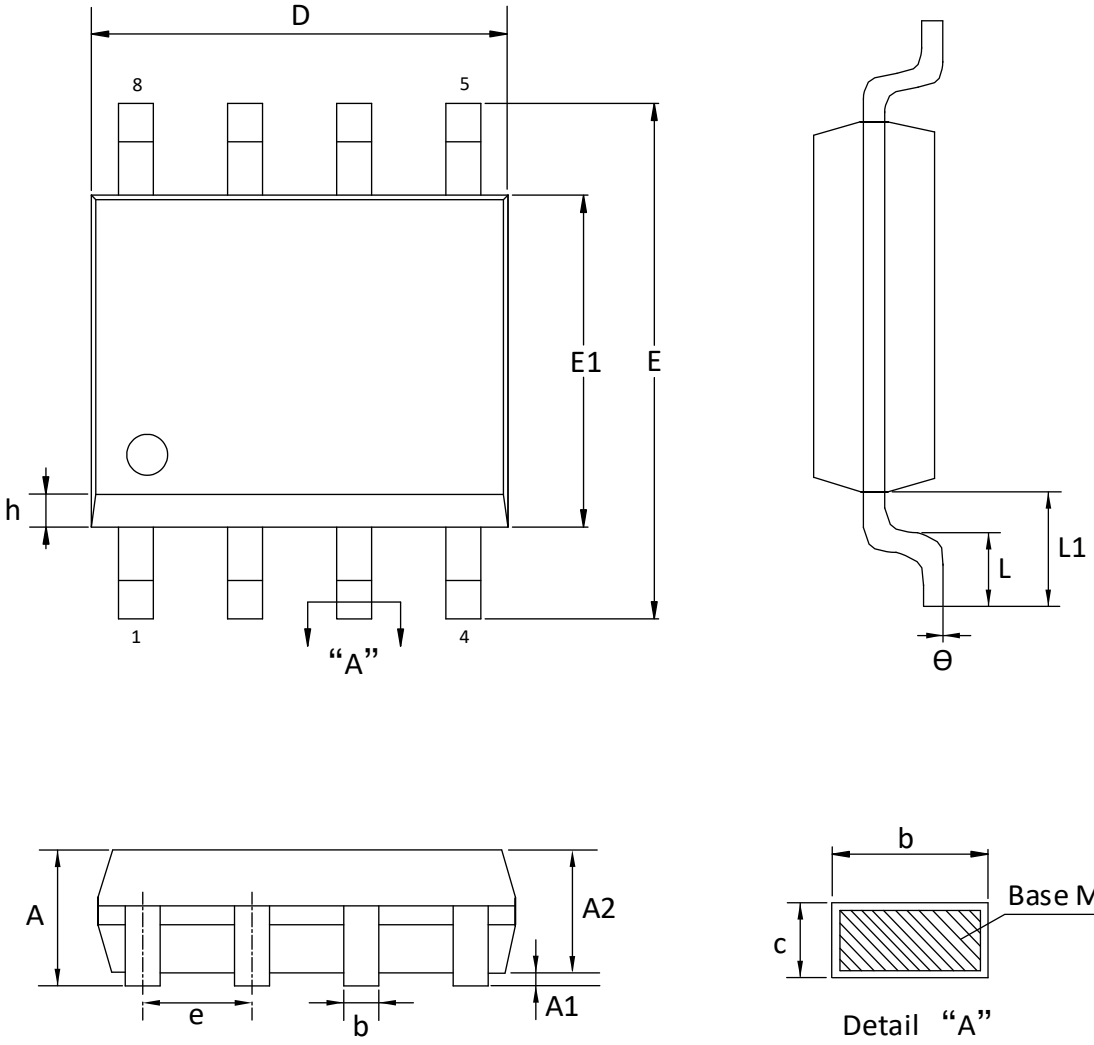


11. ORDERING INFORMATION



12. PACKAGE INFORMATION

12.1 Package SOP8 150 MIL



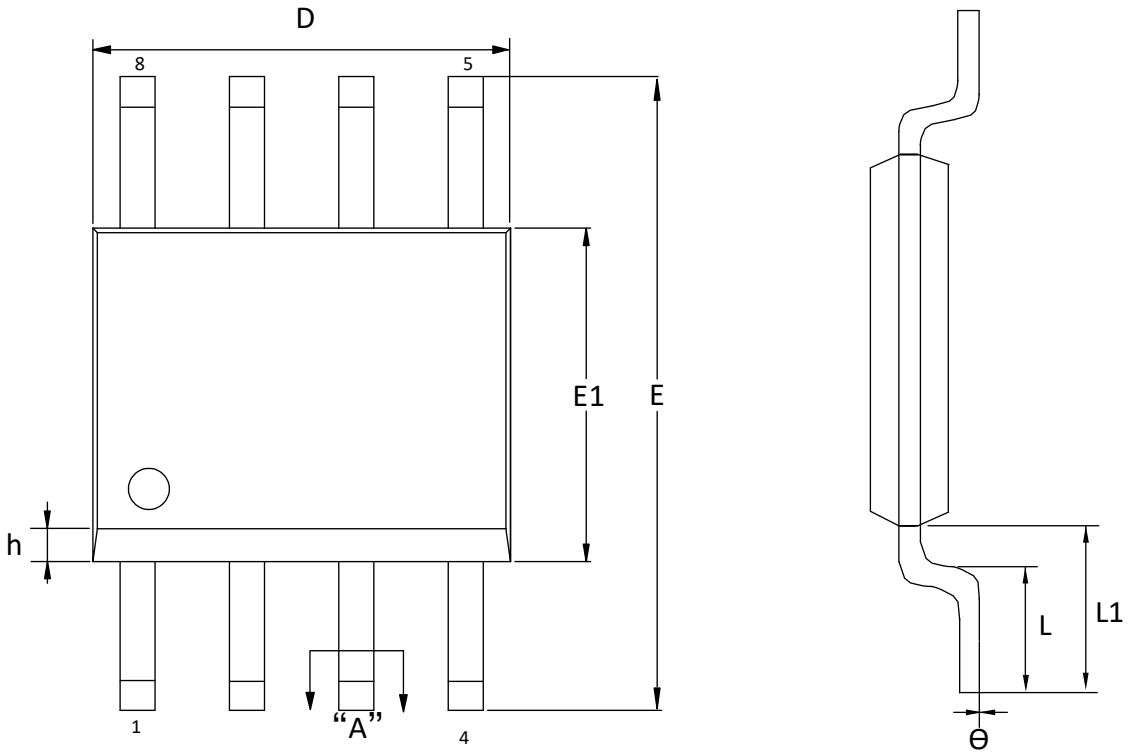
Dimensions

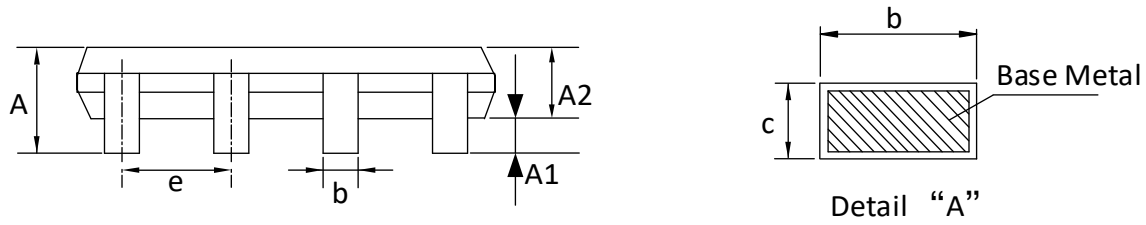
Symbol / Unit		A	A1	A2	b	c	D	E	E1	e	L	L1	h	θ
mm	Min	1.35	0.05	1.35	0.38	0.17	4.80	5.80	3.80	1.27	0.50	1.04	0.30	0°
	Nom	1.55	0.10	1.40	-	-	4.90	6.00	3.90		0.60		0.40	-
	Max	1.65	0.15	1.50	0.51	0.25	5.00	6.20	4.00		0.80		0.50	8°

Note:

1. Both the package length and width do not include the mold FLASH.
2. Seating plane: Max. 0.25mm.

12.2 Package TSSOP8





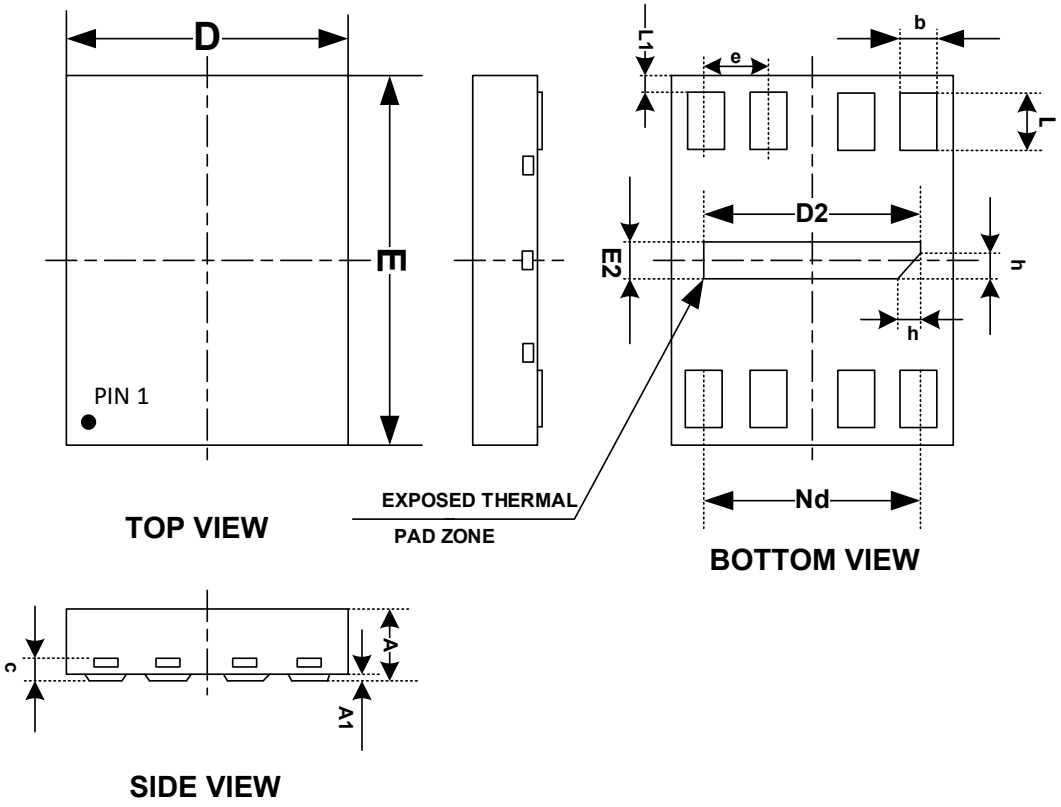
Dimensions

Symbol / Unit		A	A1	A2	b	c	D	E	E1	e	L	L1	h	θ
mm	Min		0.05	0.8	0.19	0.09	2.90	6.20	4.30	0.65	0.45	1.00		0°
	Nom			1.00	-	-	3.00	6.40	4.40		0.60			-
	Max	1.2	0.15	1.05	0.30	0.20	3.10	6.60	4.50		0.75			8°

Note:

1. Both the package length and width do not include the mold FLASH.
2. Seating plane: Max. 0.25mm.

12.3 Package USON (3x2x0.45)



Dimensions

Symbol Unit		A	A1	b	c	D	D2	e	Nd	E	E2	L	L1	h
mm	Min	0.4	0	0.2	0.1	1.9	1.5	0.50BSC	1.50BSC	2.9	0.1	0.3	0.05	0.05
	Nom	0.45	0.02	0.25	0.15	2	1.6			3	0.2	0.35	0.1	0.15
	Max	0.5	0.05	0.3	0.2	2.1	1.7			3.1	0.3	0.4	0.15	0.25

13. REVISION HISTORY

Version No	Description	Page	Date
1.0	Initial Release	All	2023-04-01

IMPORTANT NOTICE

UCUN Technology reserves the right to make changes, corrections or modifications without further notice to any products or this document here in. UCUN Technology does not assume any responsibility for use of any its products for any particular purpose, nor does UCUN Technology assume any liability arising out of the application or use of any its products or circuits. UCUN Technology does not convey any license under its patent rights or other rights nor the rights of others.